Figure 1 PRIOR ART

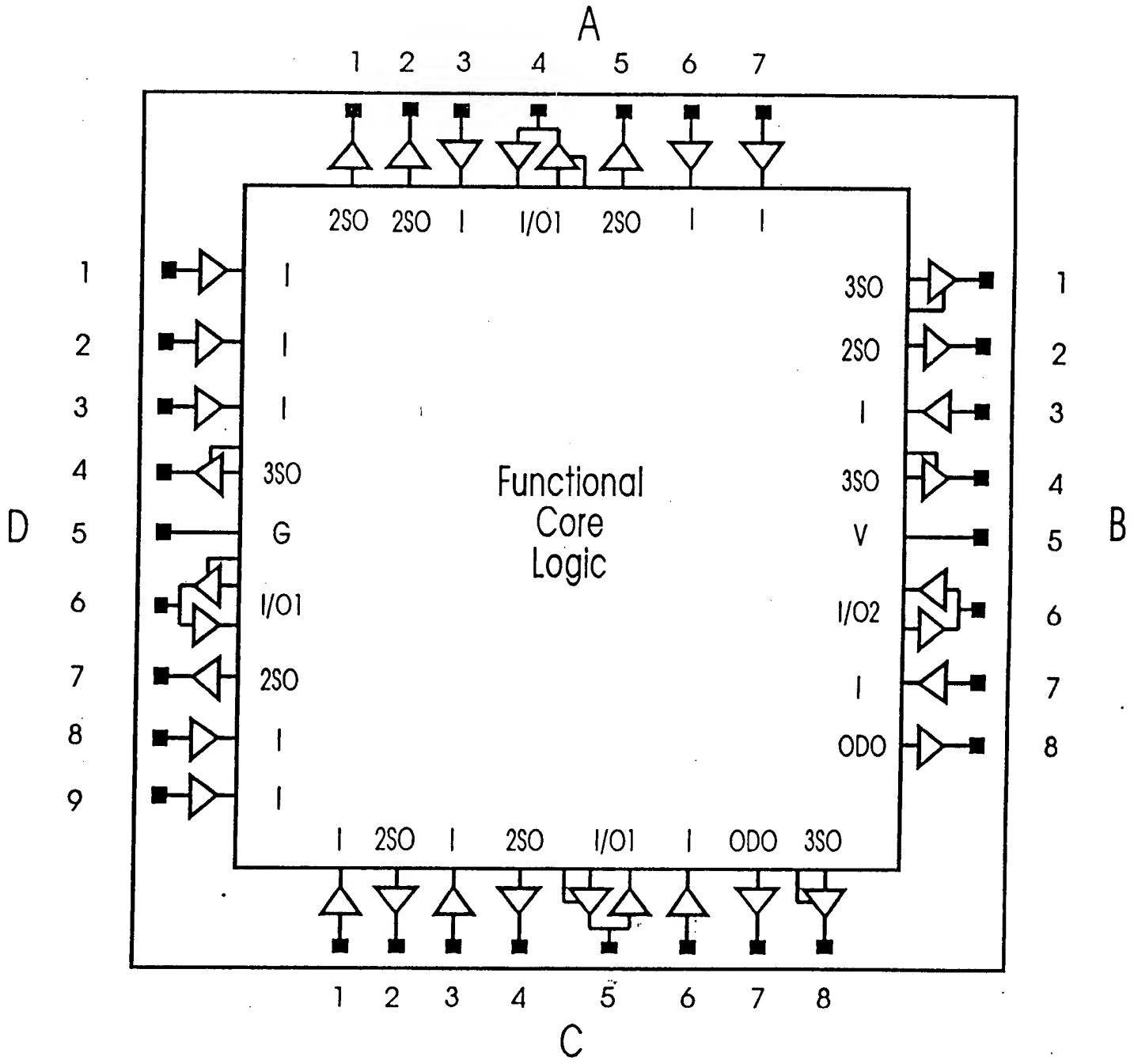


Figure 2

PRIOR ART

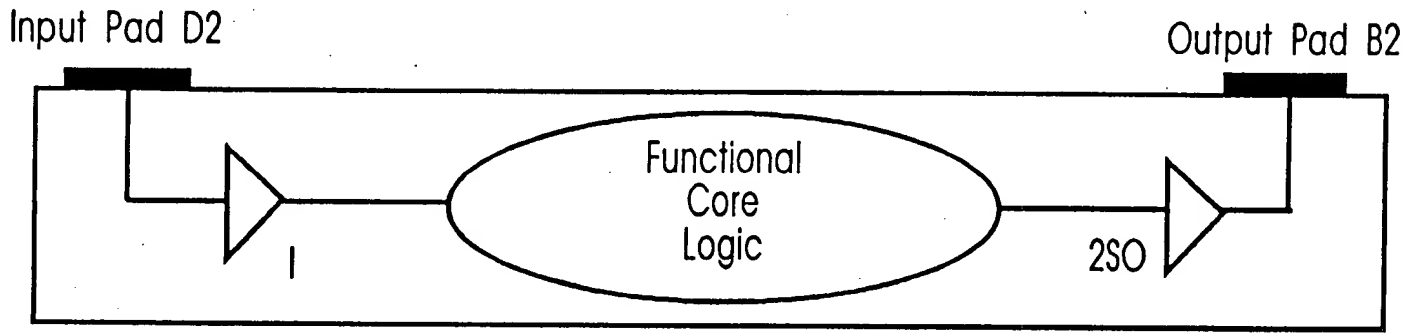


Figure 3A PRIOR ART

Figure 3B PRIOR ART

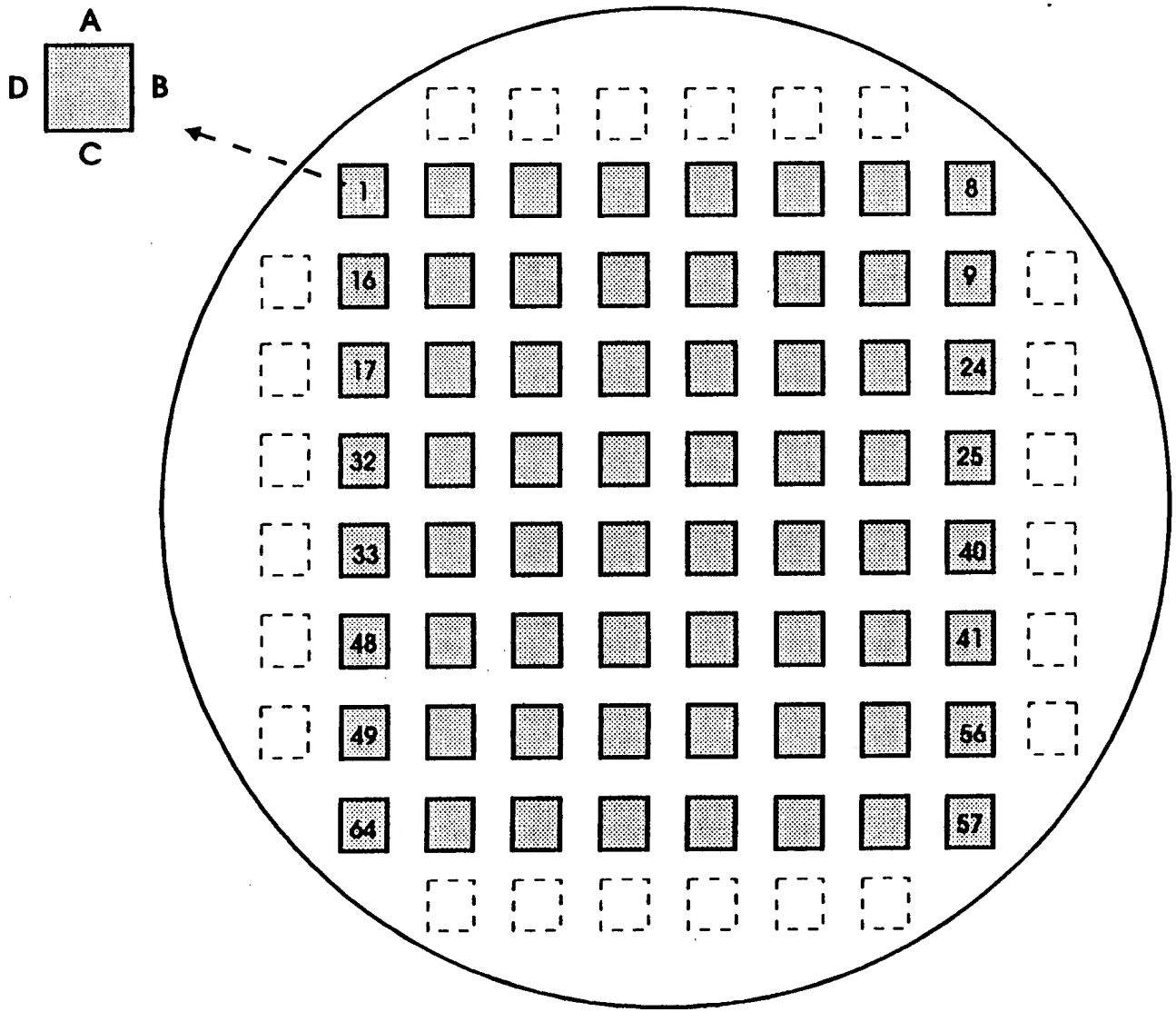


Figure 4 PRIOR ART

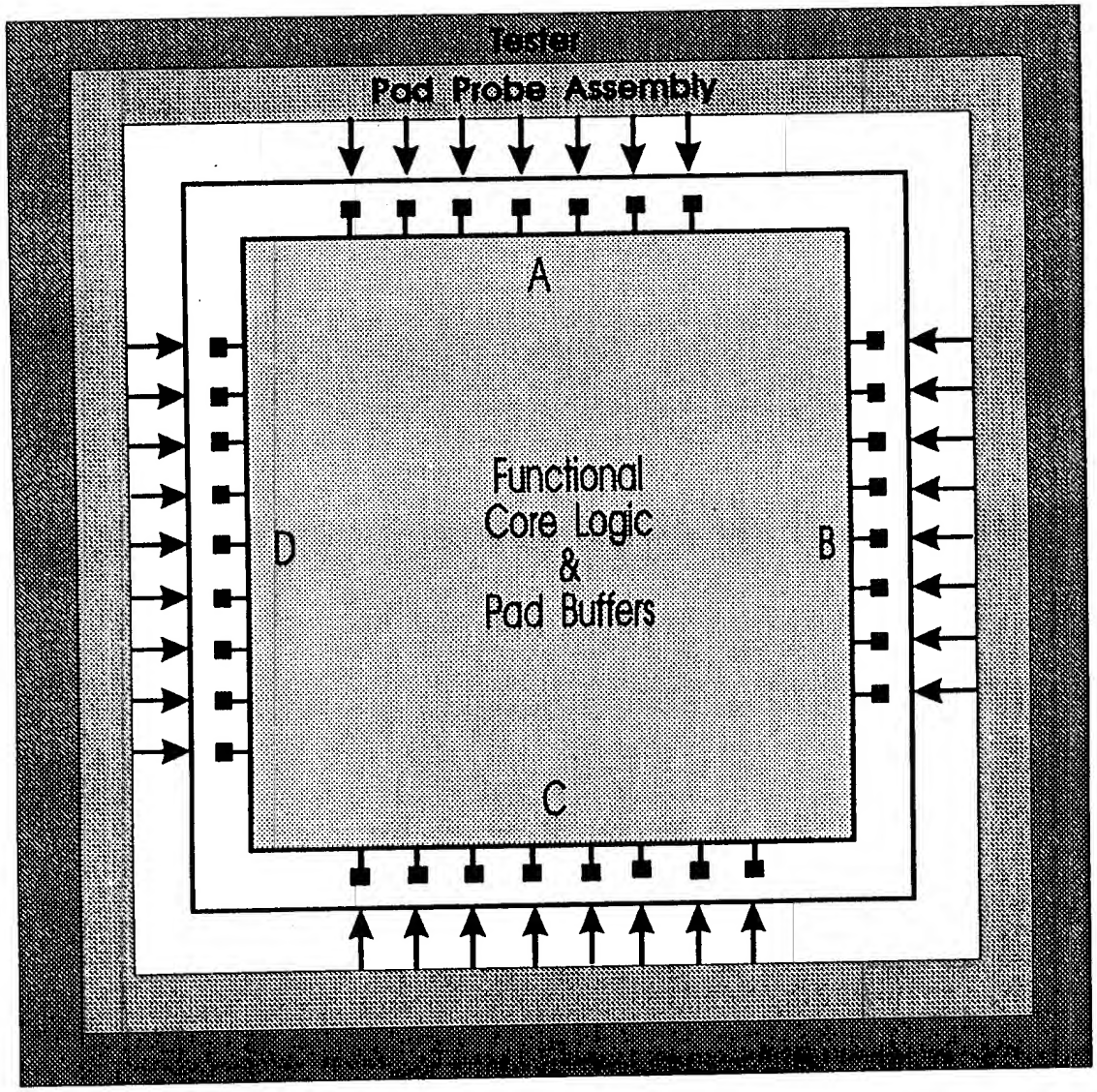


Figure 5

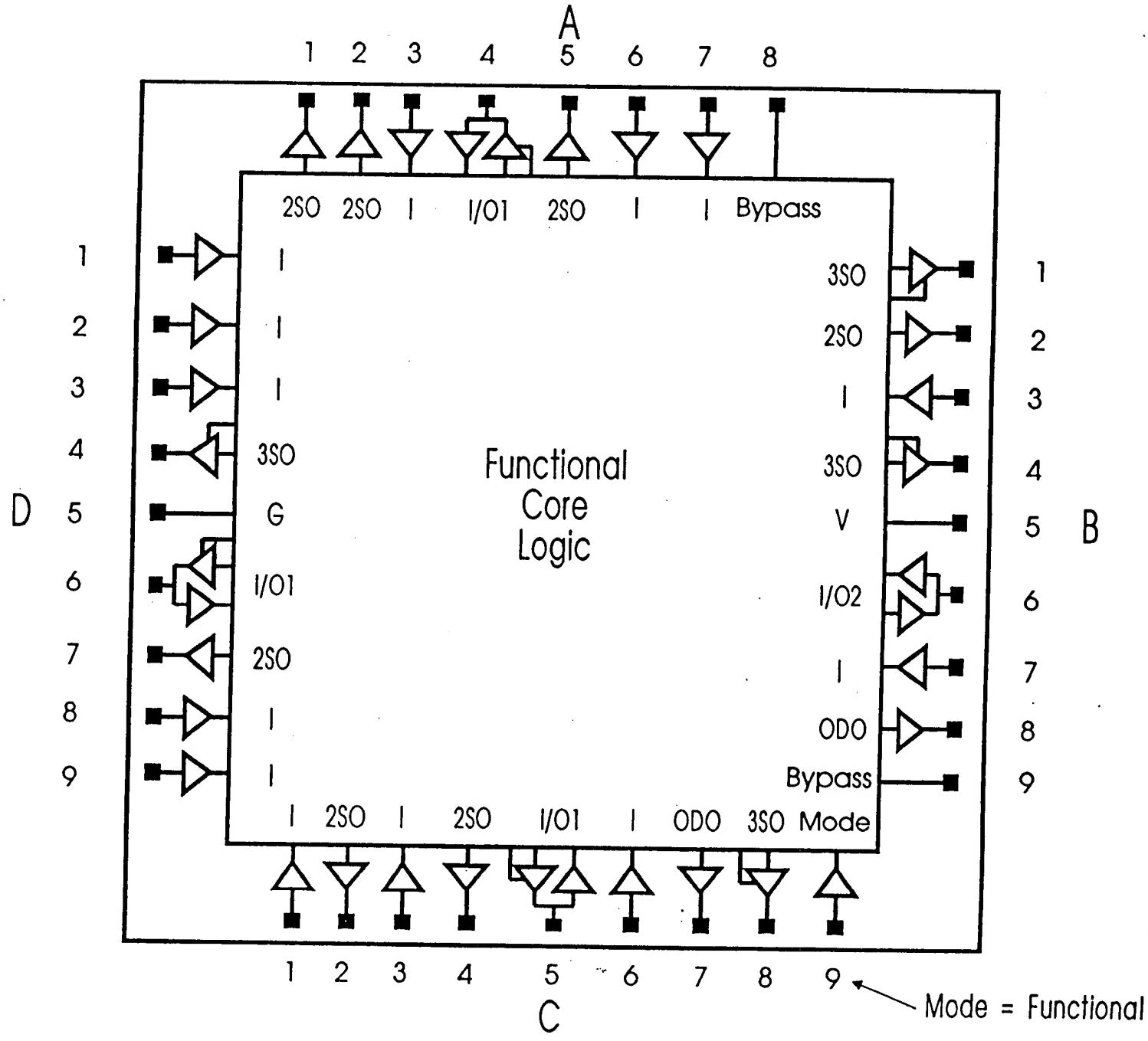

A
1 2 3 4 5 6 7 8
2SO 2SO I I/O1 2SO I I Bypass
1
2
3
4
D 5
6
7
8
9
I
I
I
3SO
G
I/O1
2SO
I
I
3SO
2SO
I
3SO
V
I/O2
I
ODO
Bypass
1
2
3
4
5 B
6
7
8
9
Functional
Core
Logic
I 2SO I 2SO I/O1 I ODO 3SO Mode
1 2 3 4 5 6 7 8 9
C
Mode = Functional

Figure 6

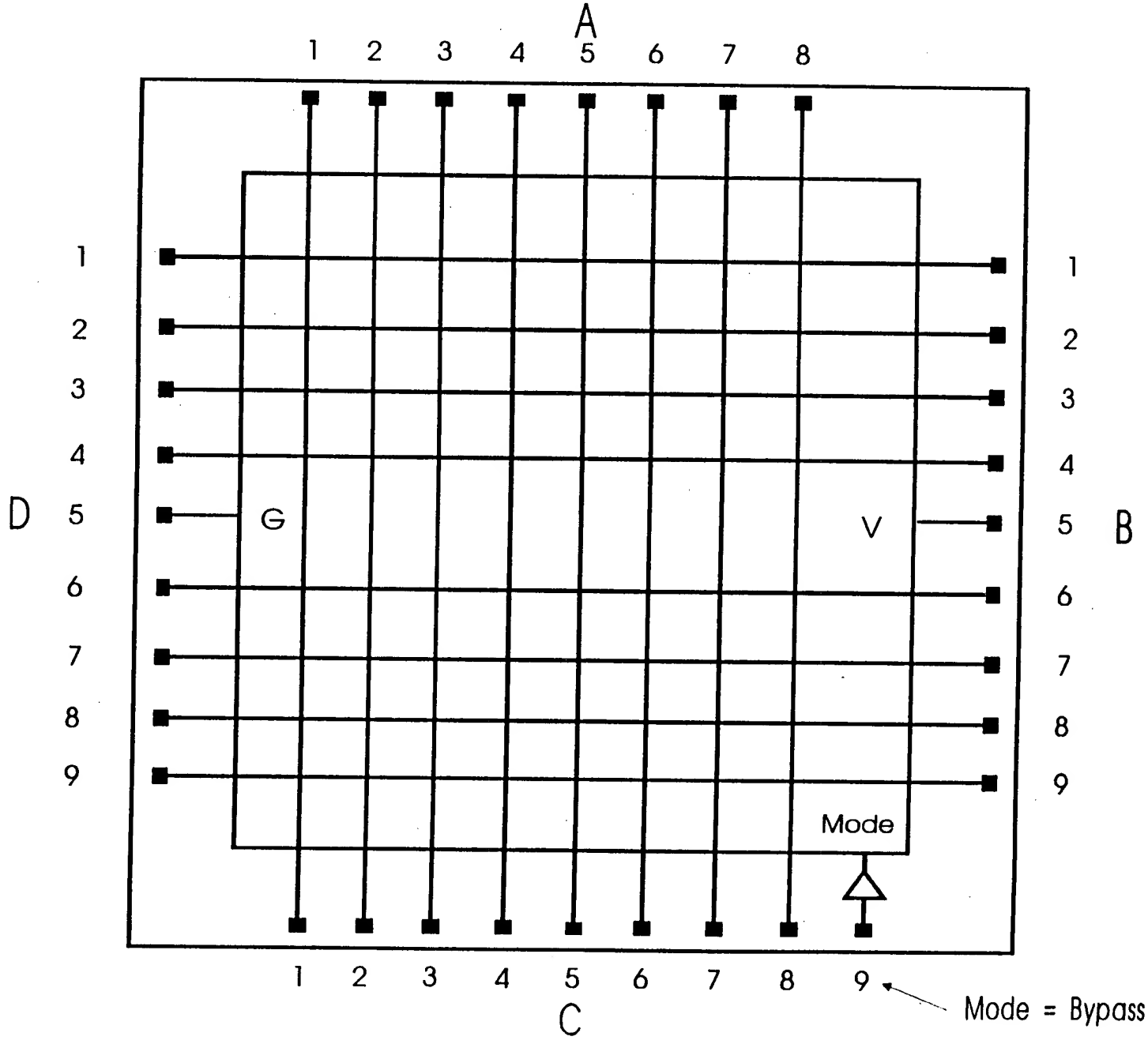

A
1 2 3 4 5 6 7 8
D
1 2 3 4 5 6 7 8 9
G
V
B
1 2 3 4 5 6 7 8 9
Mode
1 2 3 4 5 6 7 8 9
C
Mode = Bypass

Figure 7A

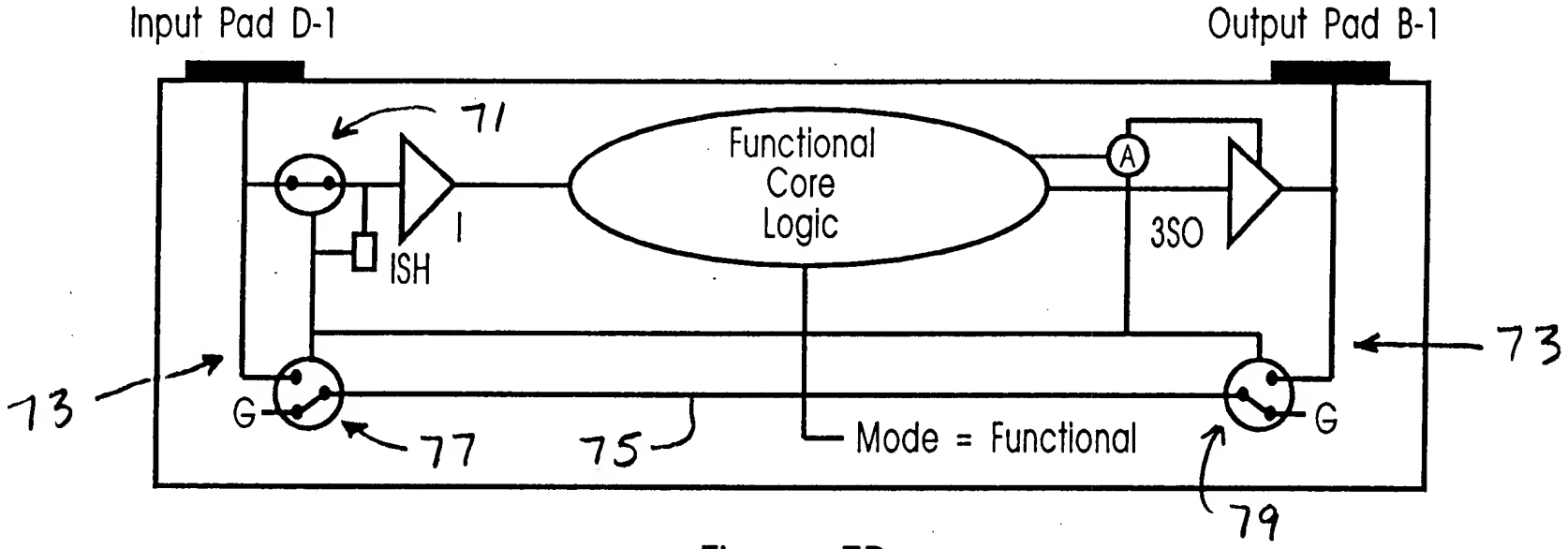


Figure 7B

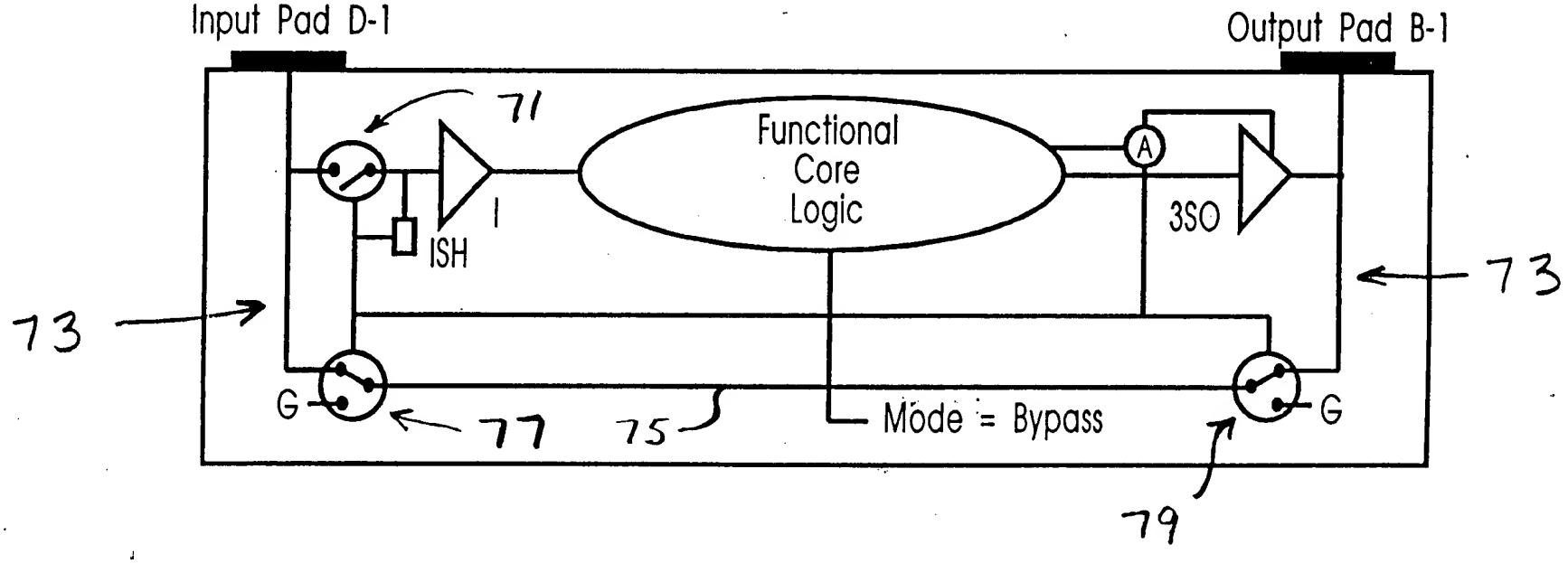


Figure 8A

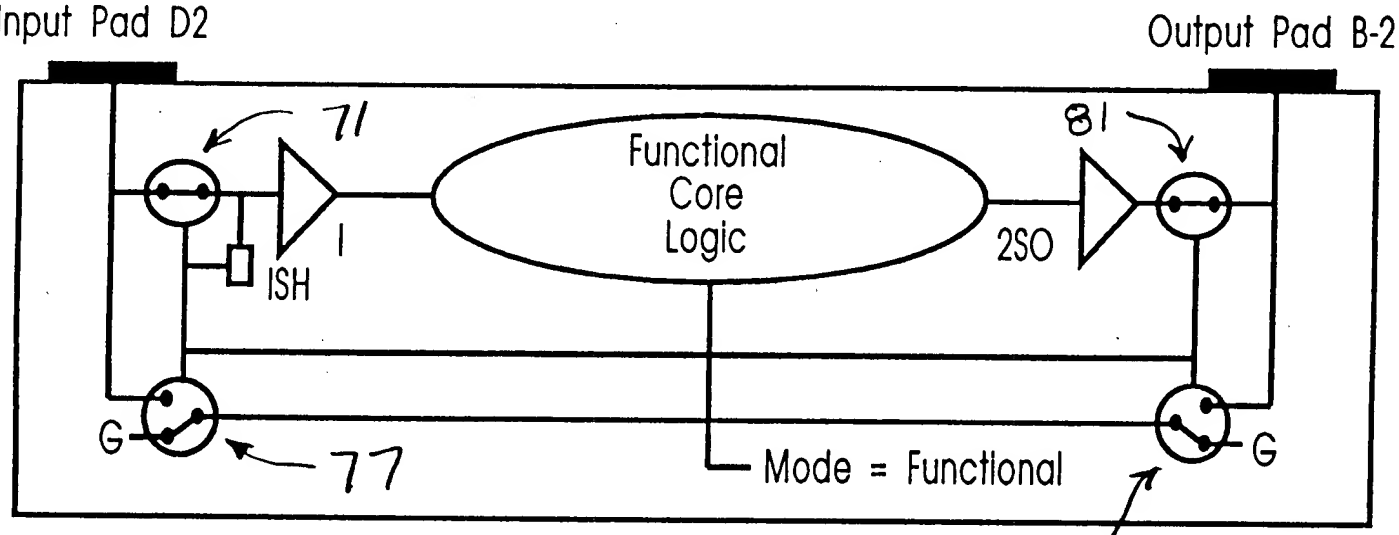


Figure 8B

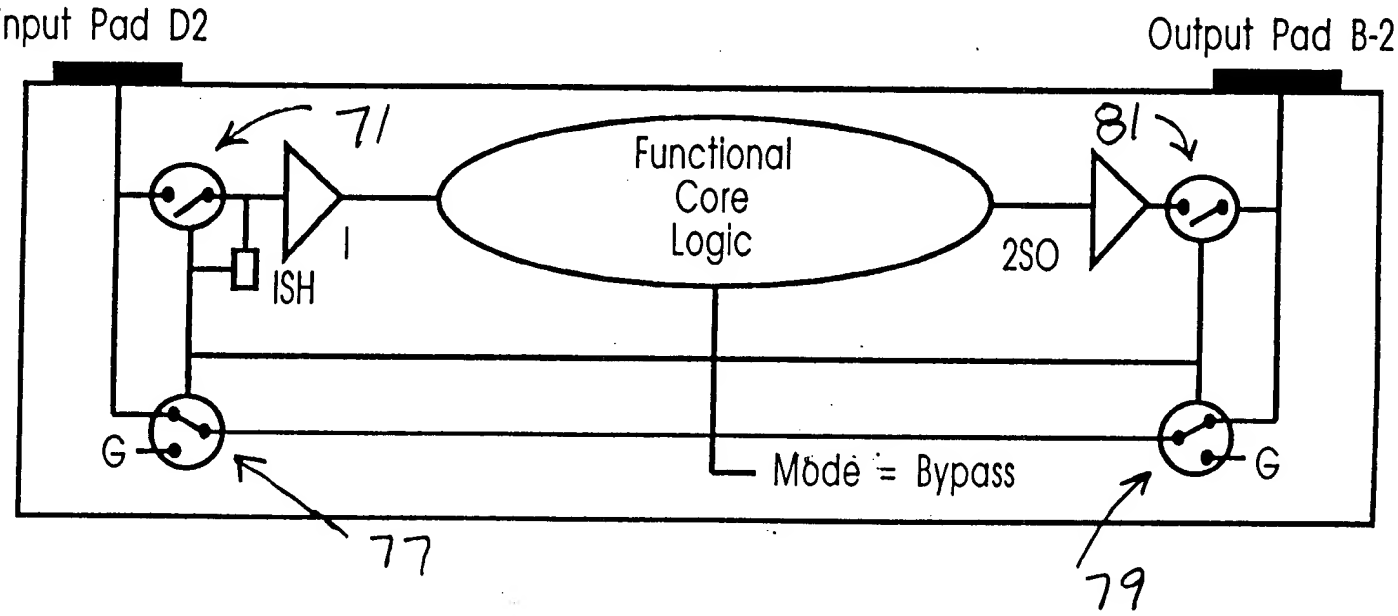


Figure 8C

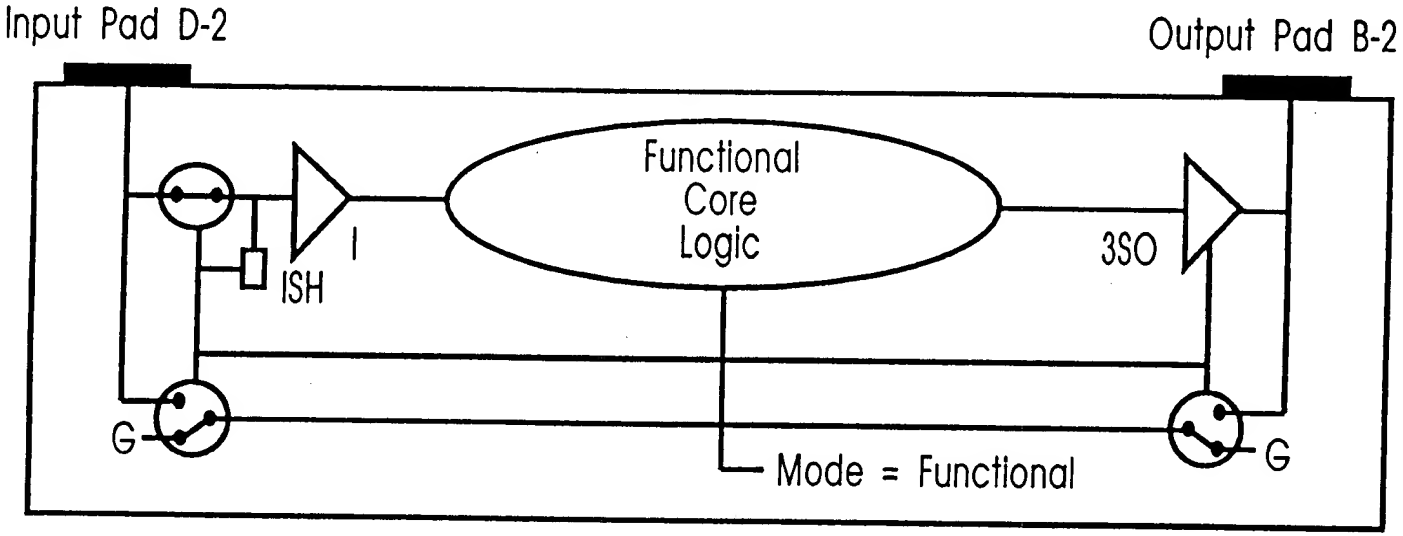


Figure 8D

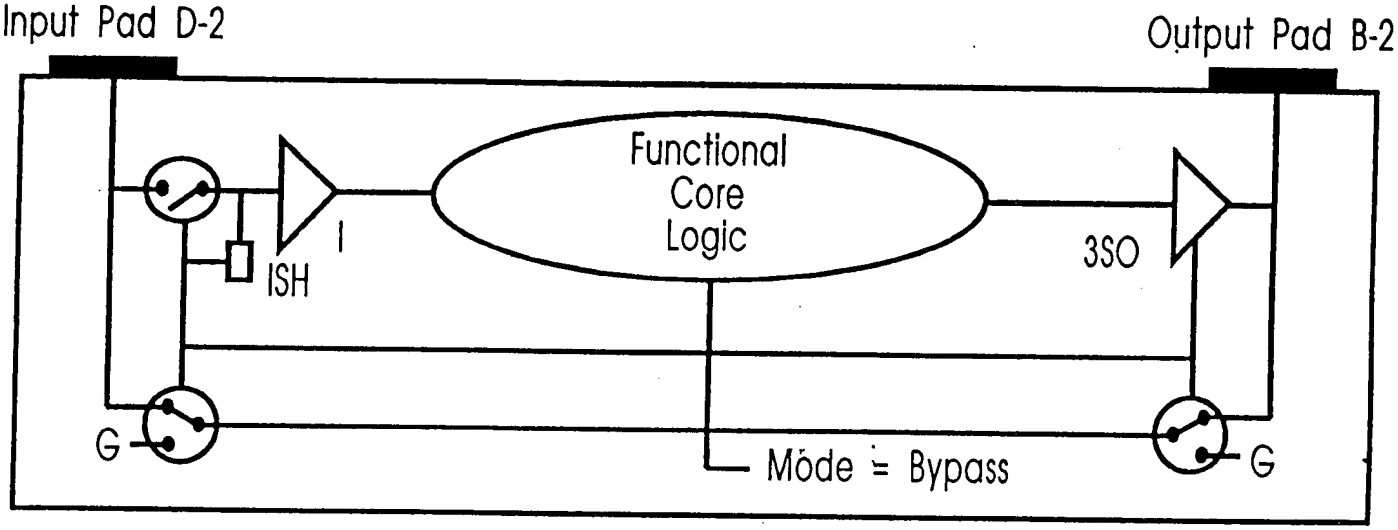


Figure 9A

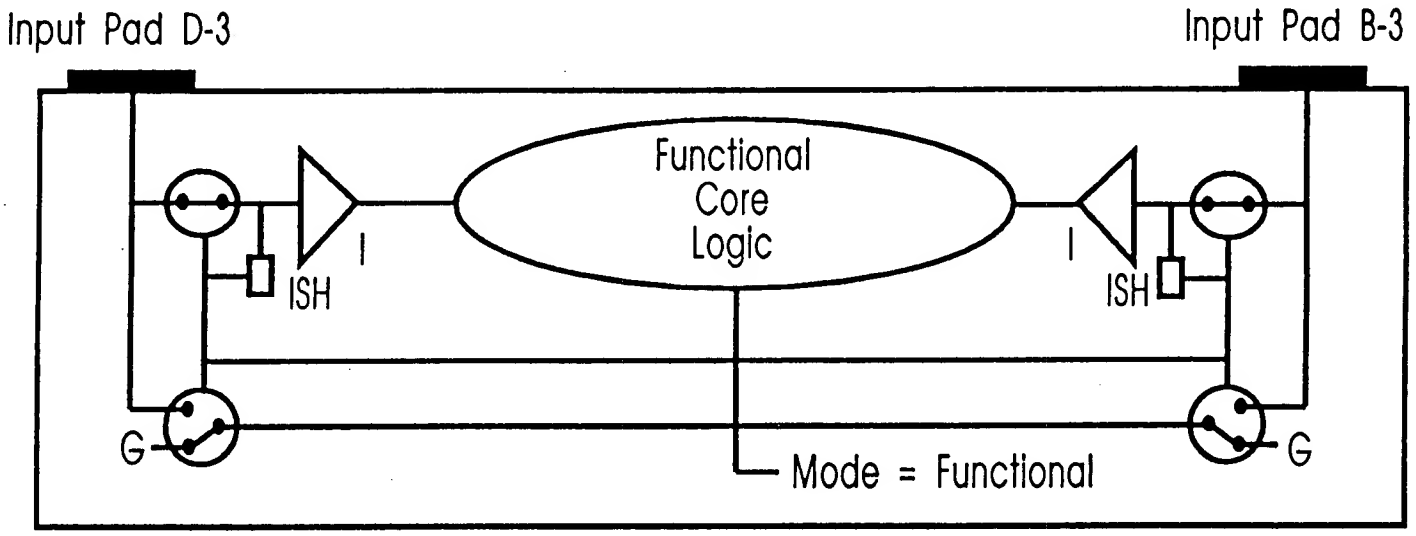


Figure 9B

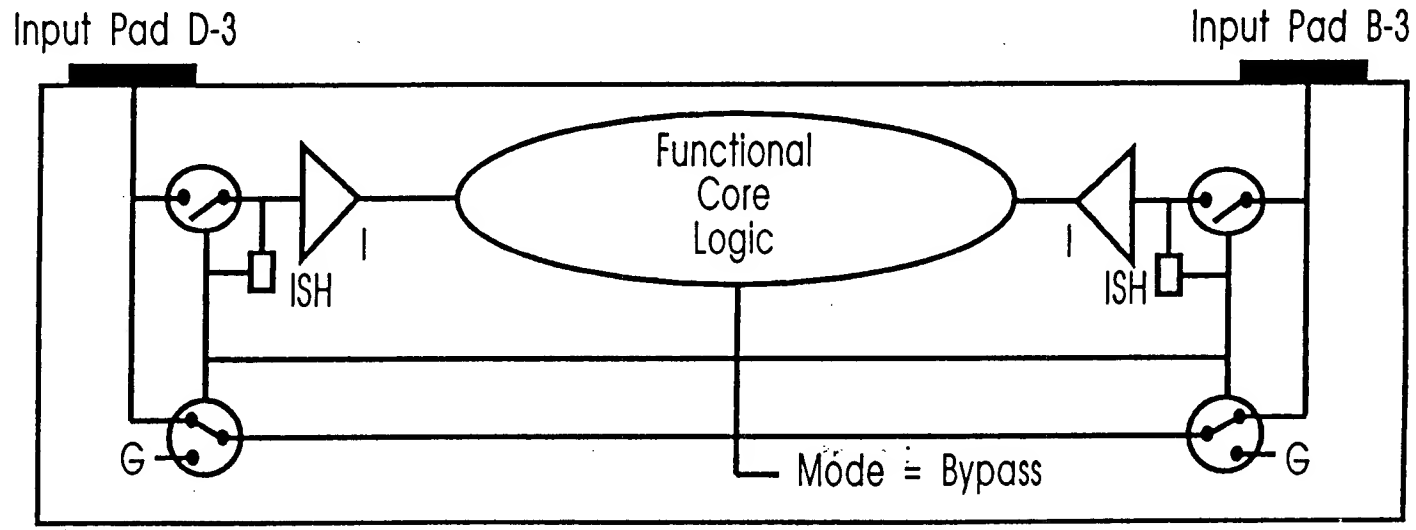


Figure 10A

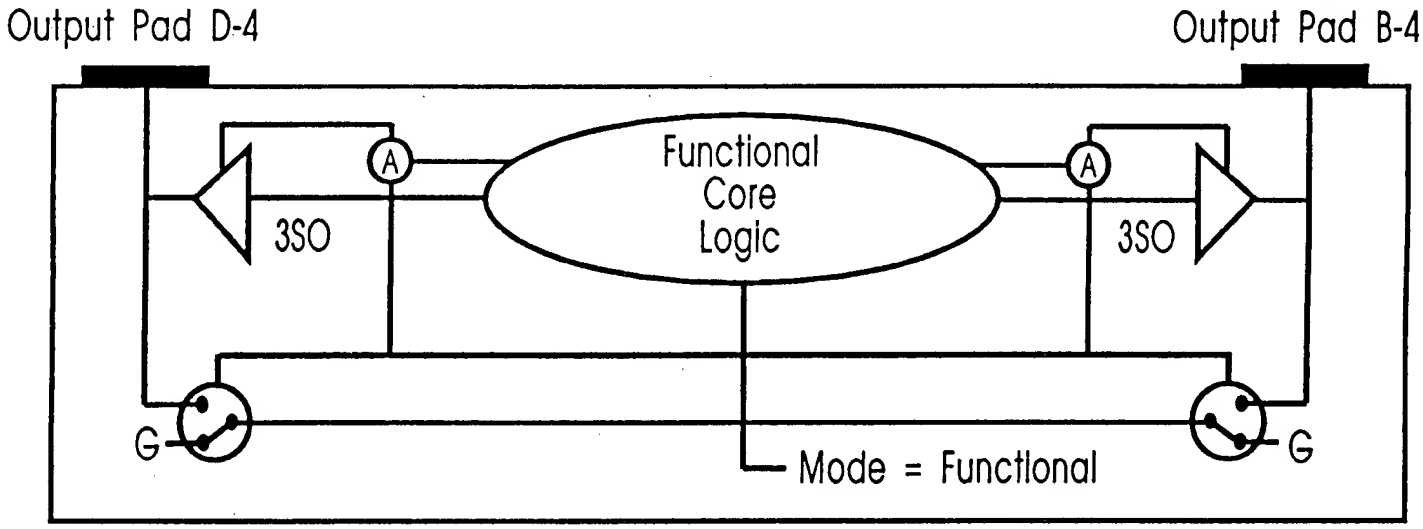


Figure 10B

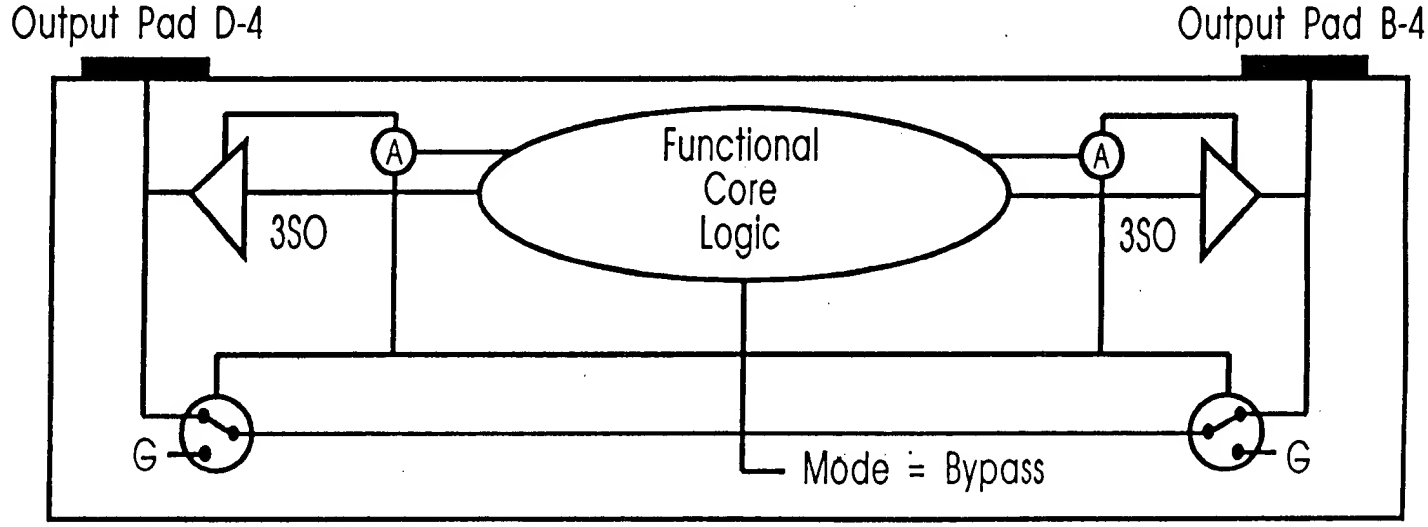


Figure 11A

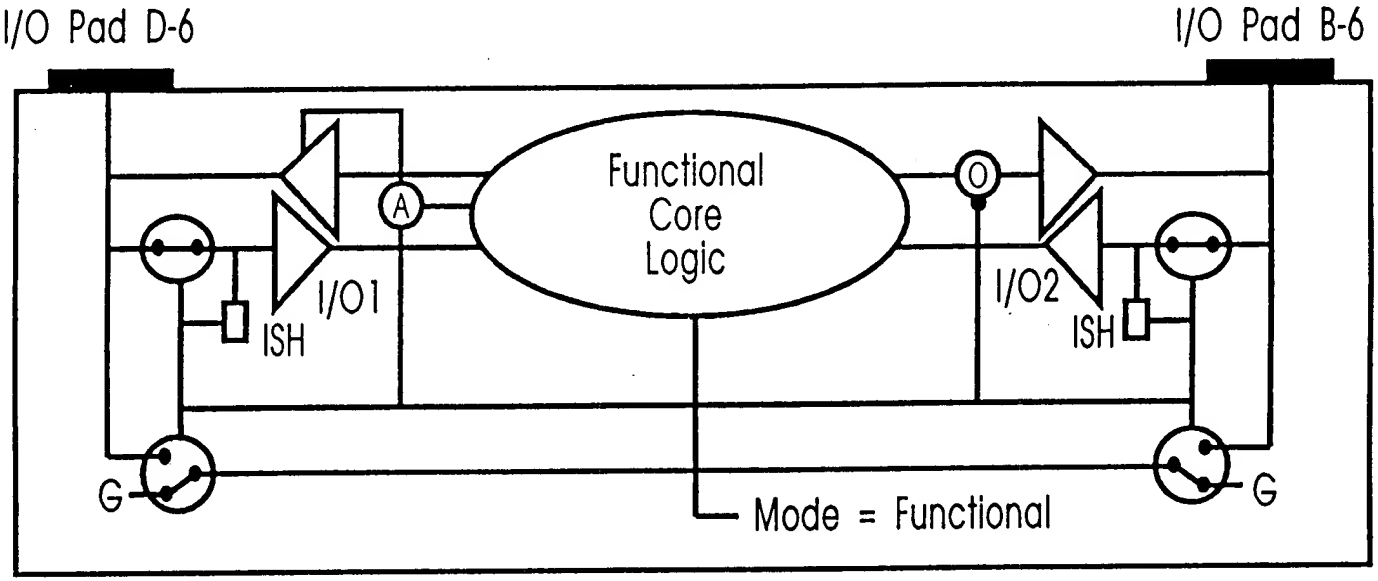


Figure 11B

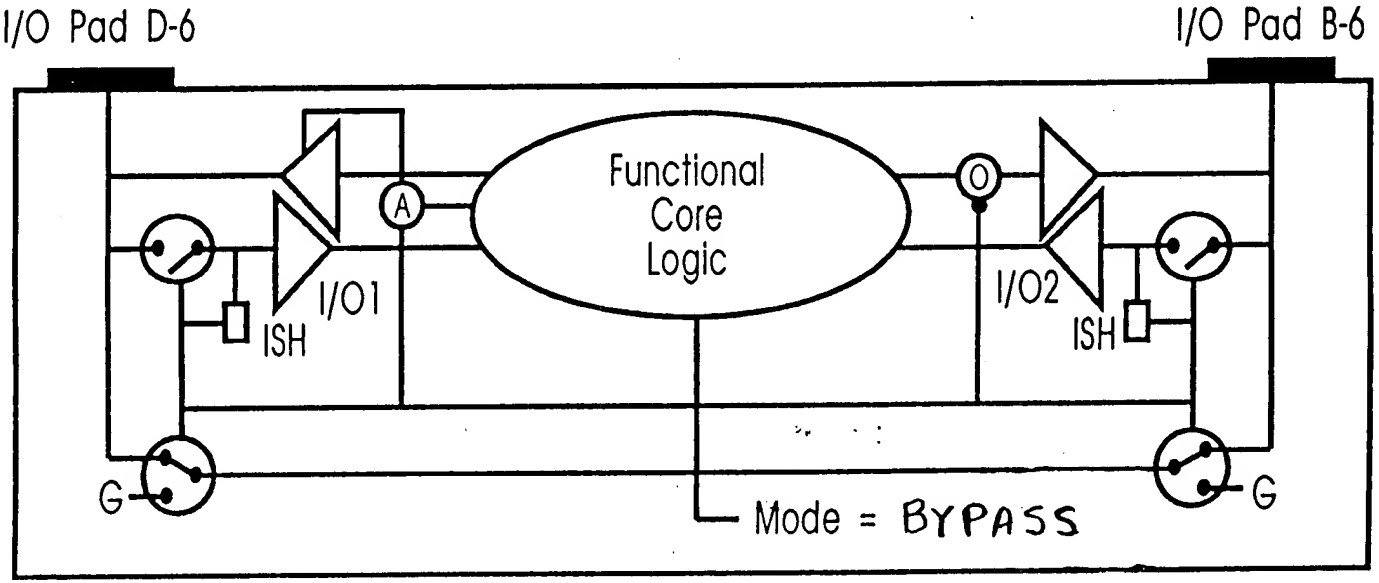


Figure 12A

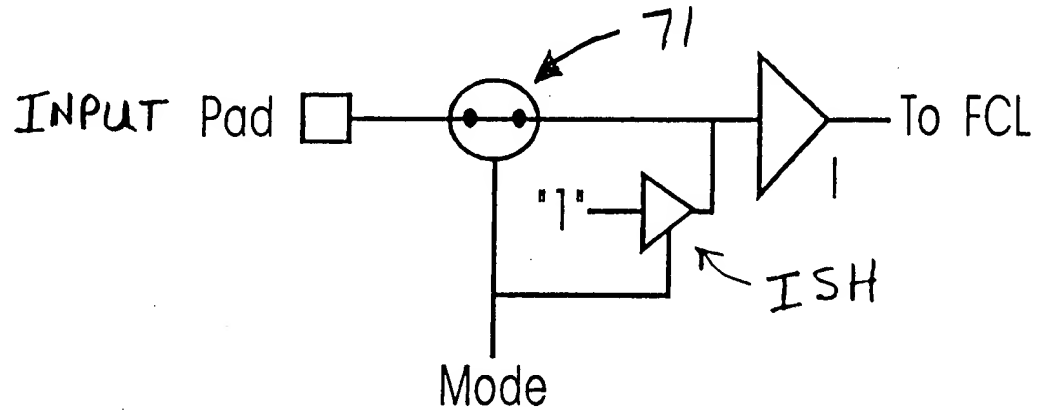


Figure 12B

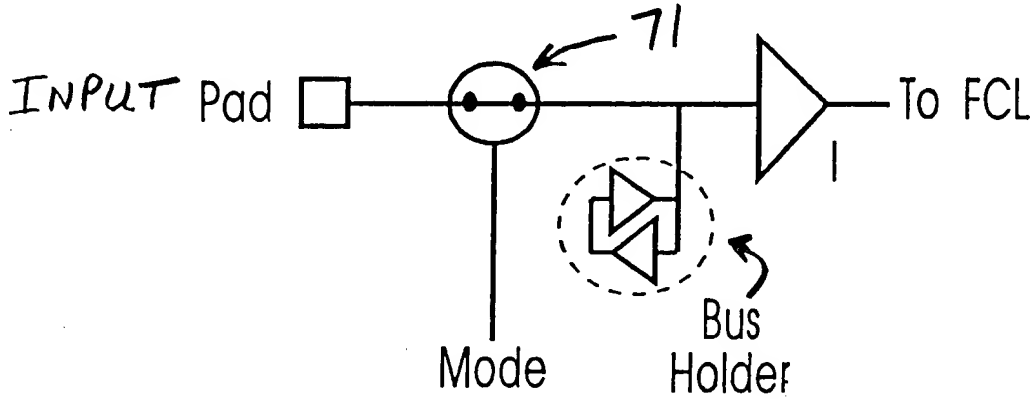


Figure 13A

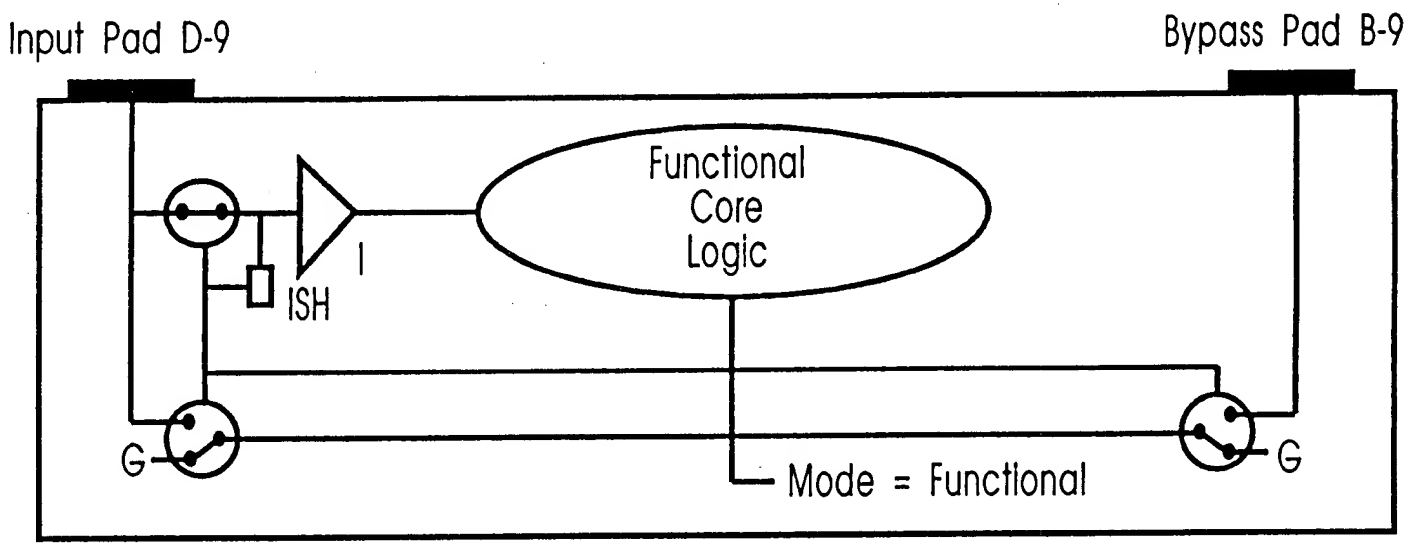


Figure 13B

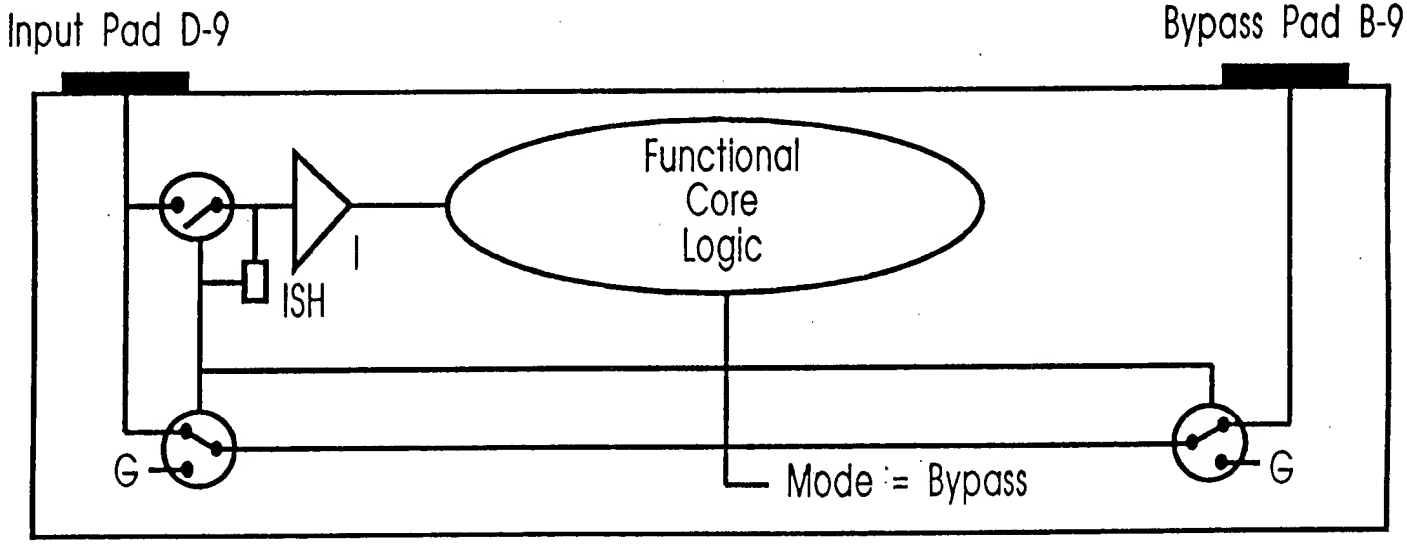


Figure 14A

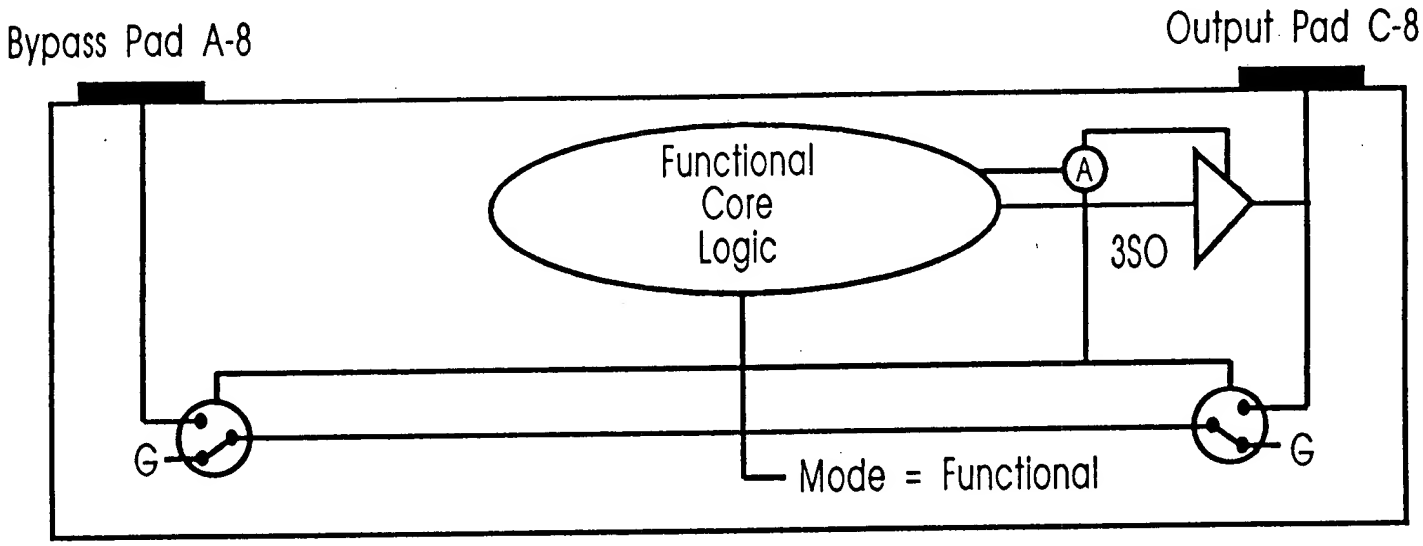


Figure 14B

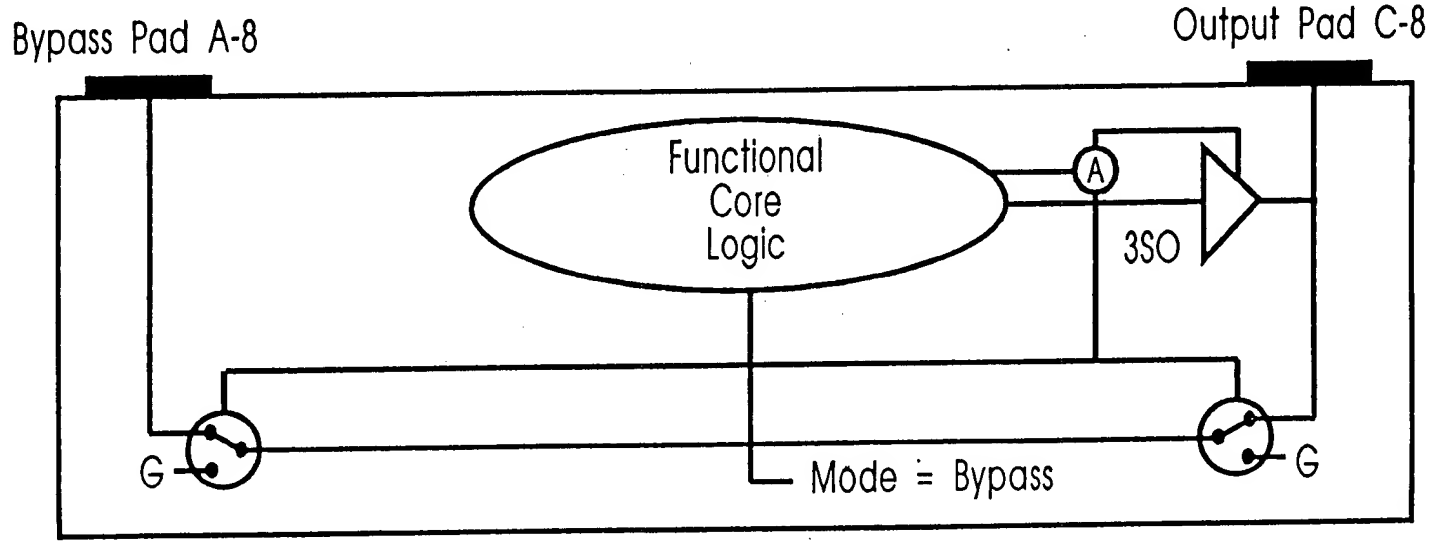


Figure 15A

Figure 15B

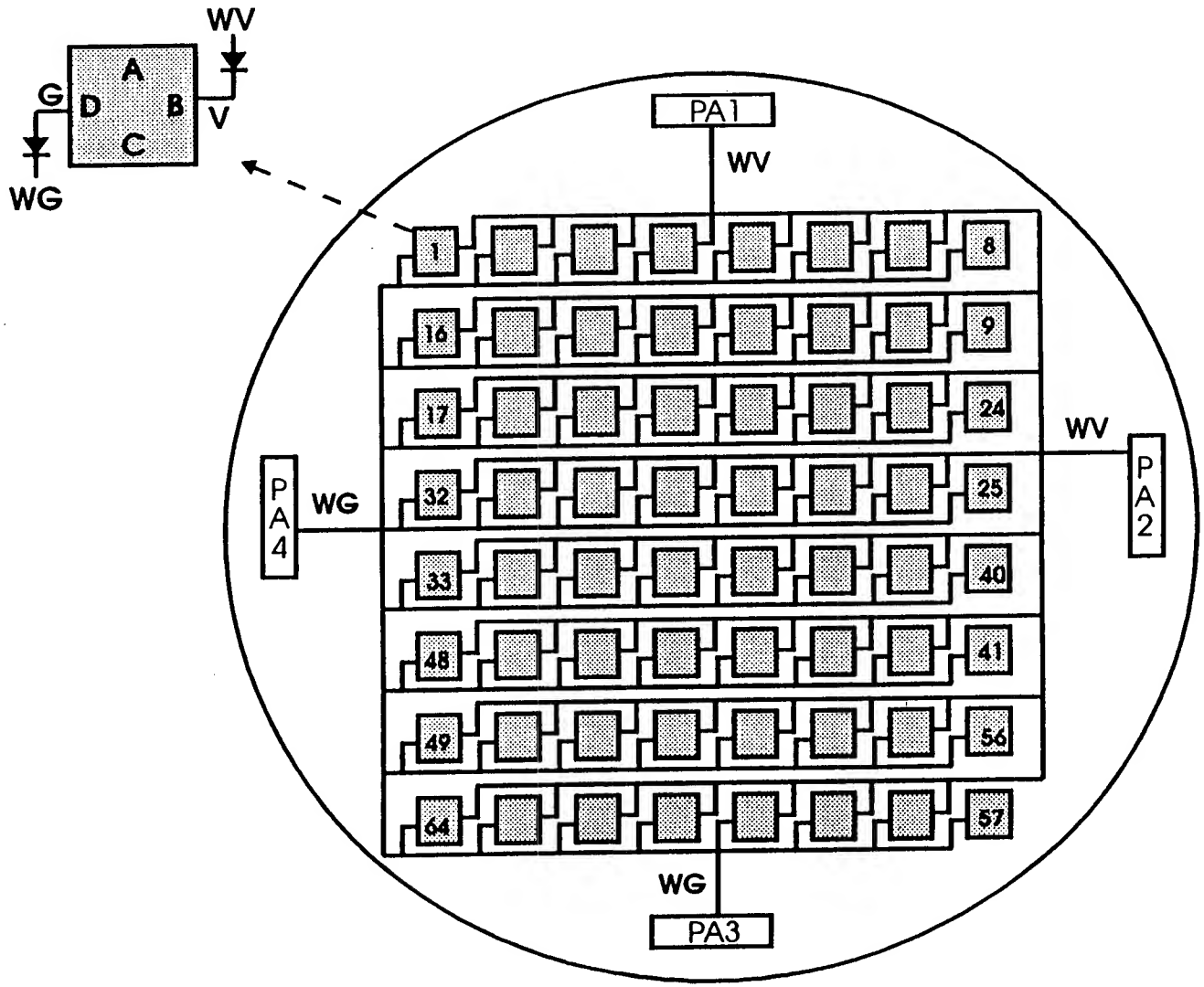


Figure 16B

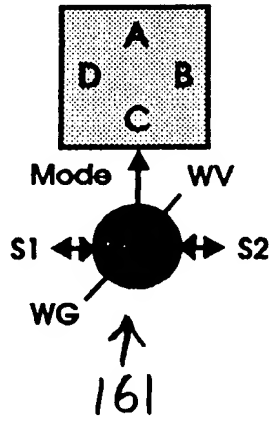


Figure 16A

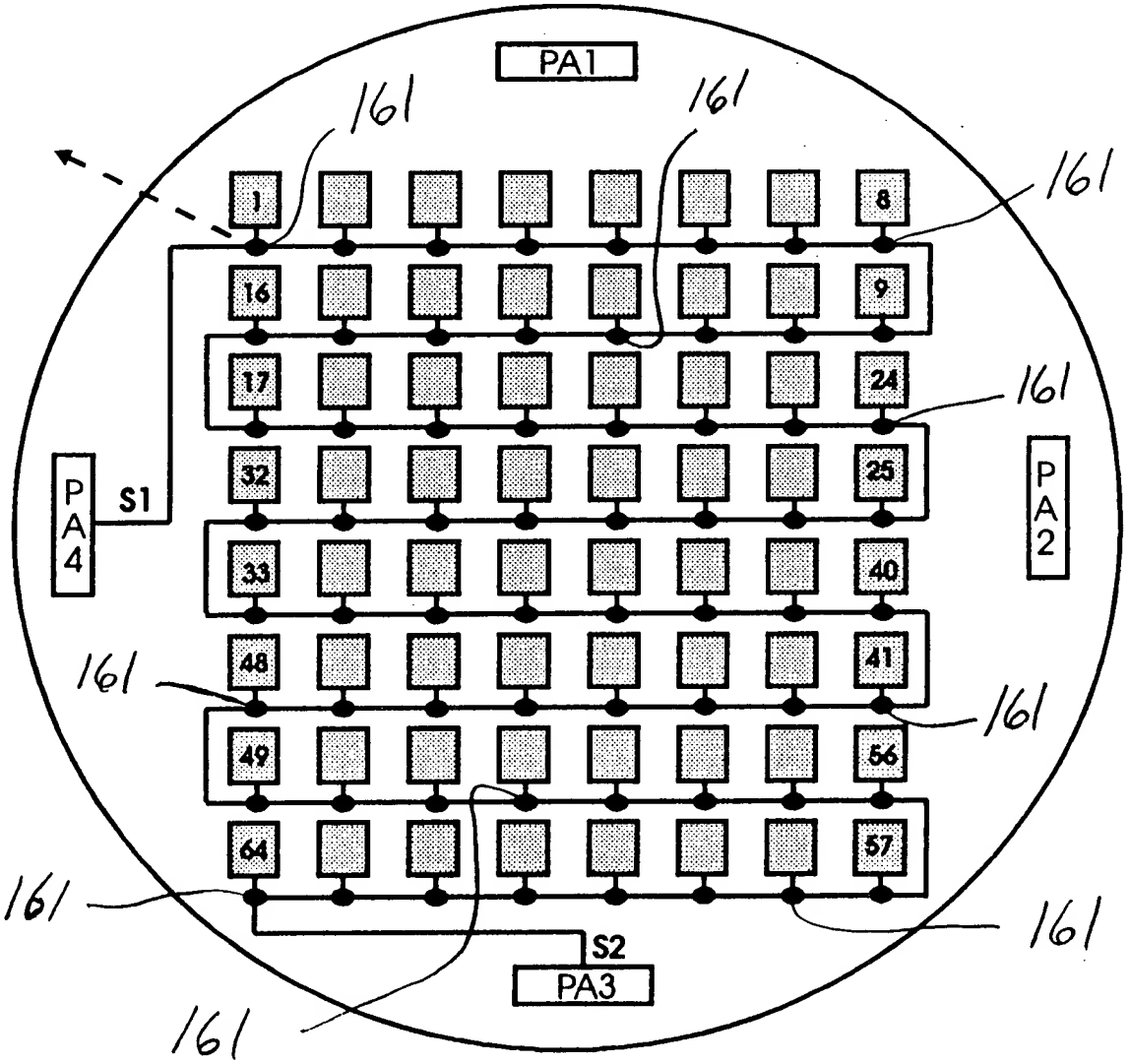


Figure 17A

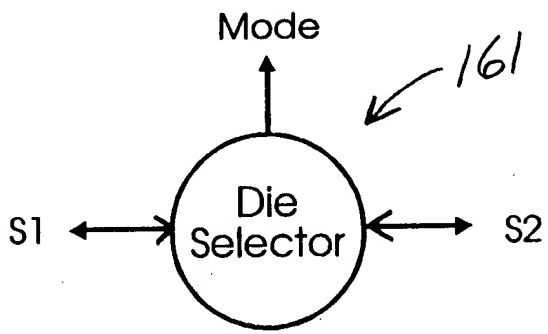


Figure 17B

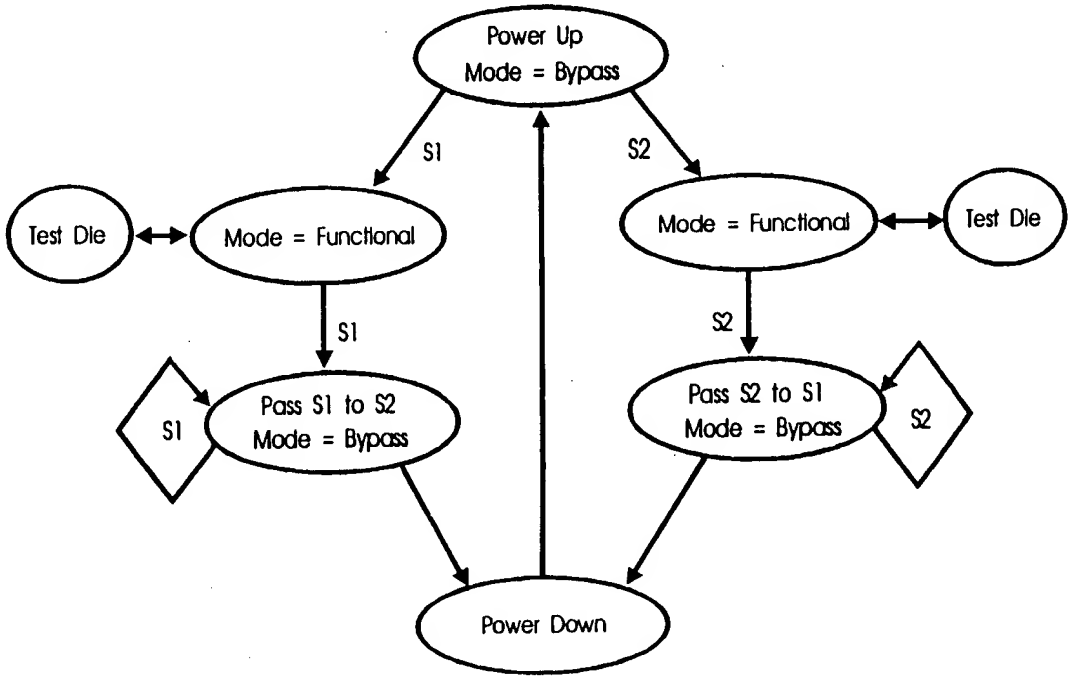


Figure 18A

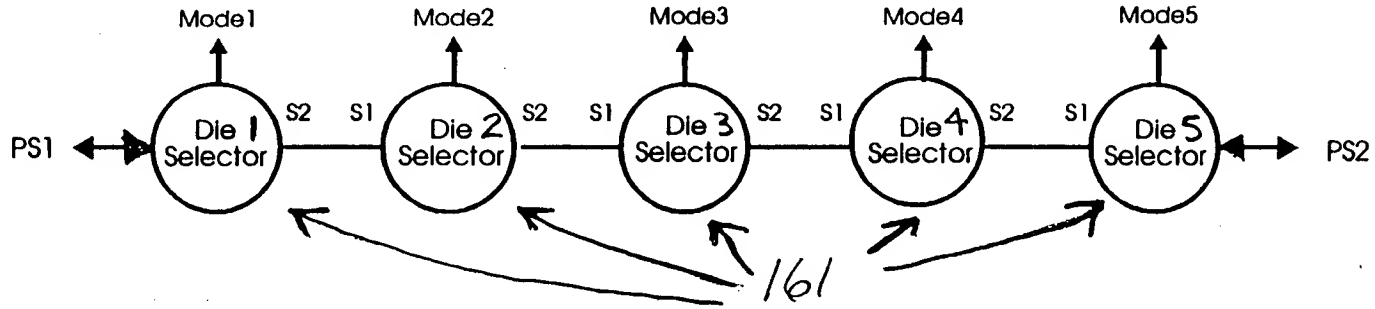


FIG. 18B

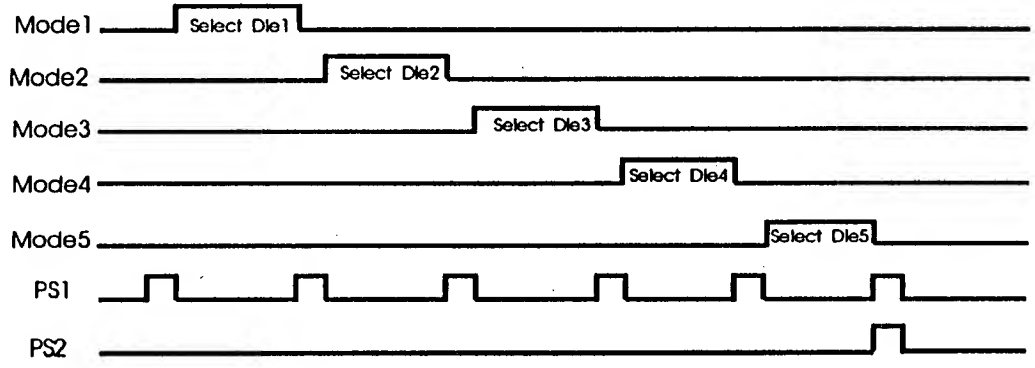


FIG. 18C

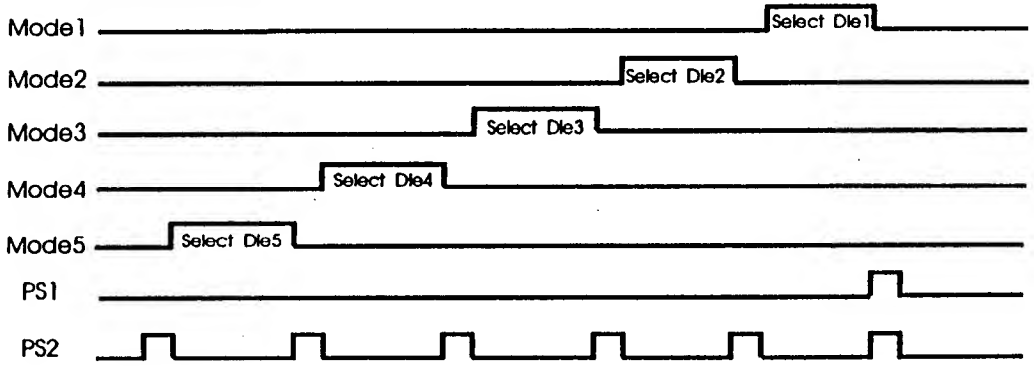


Figure 19A

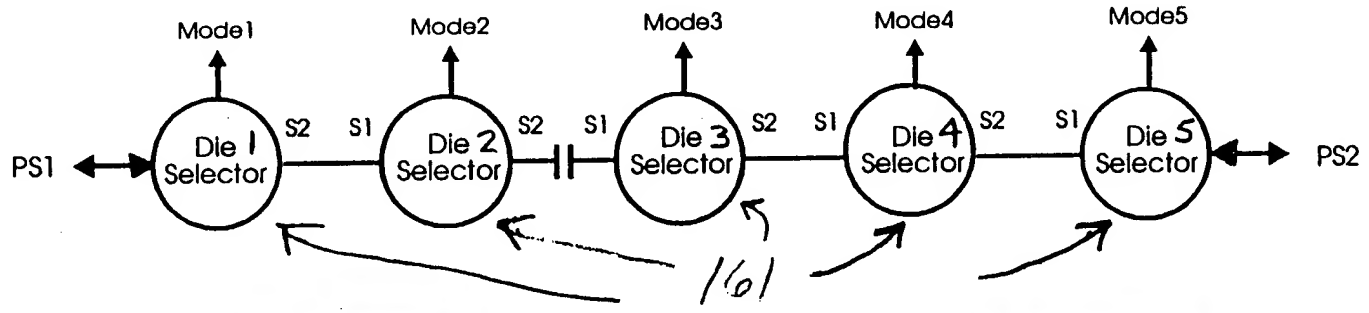


FIG. 19B

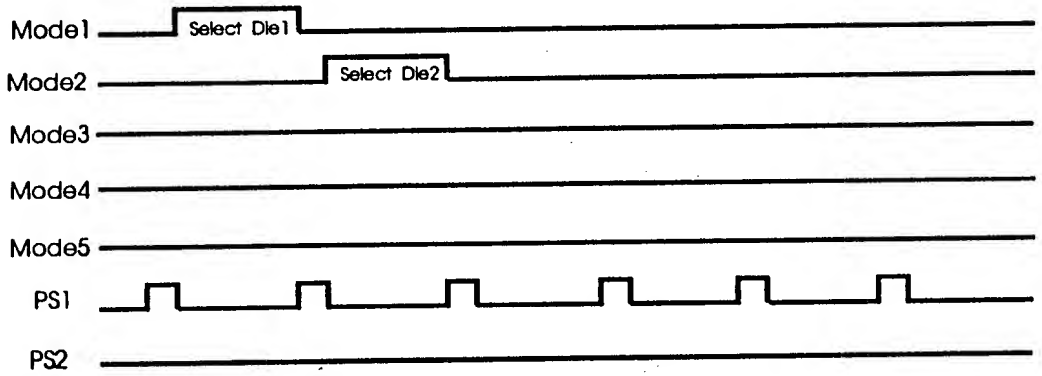


FIG. 19C

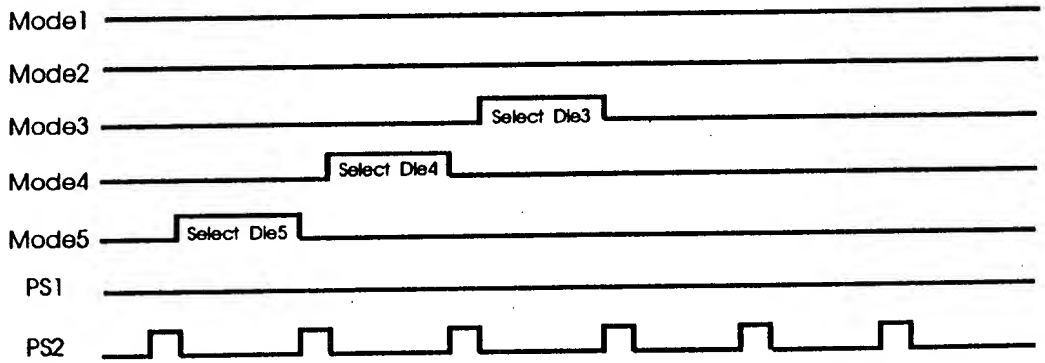


Figure 19D

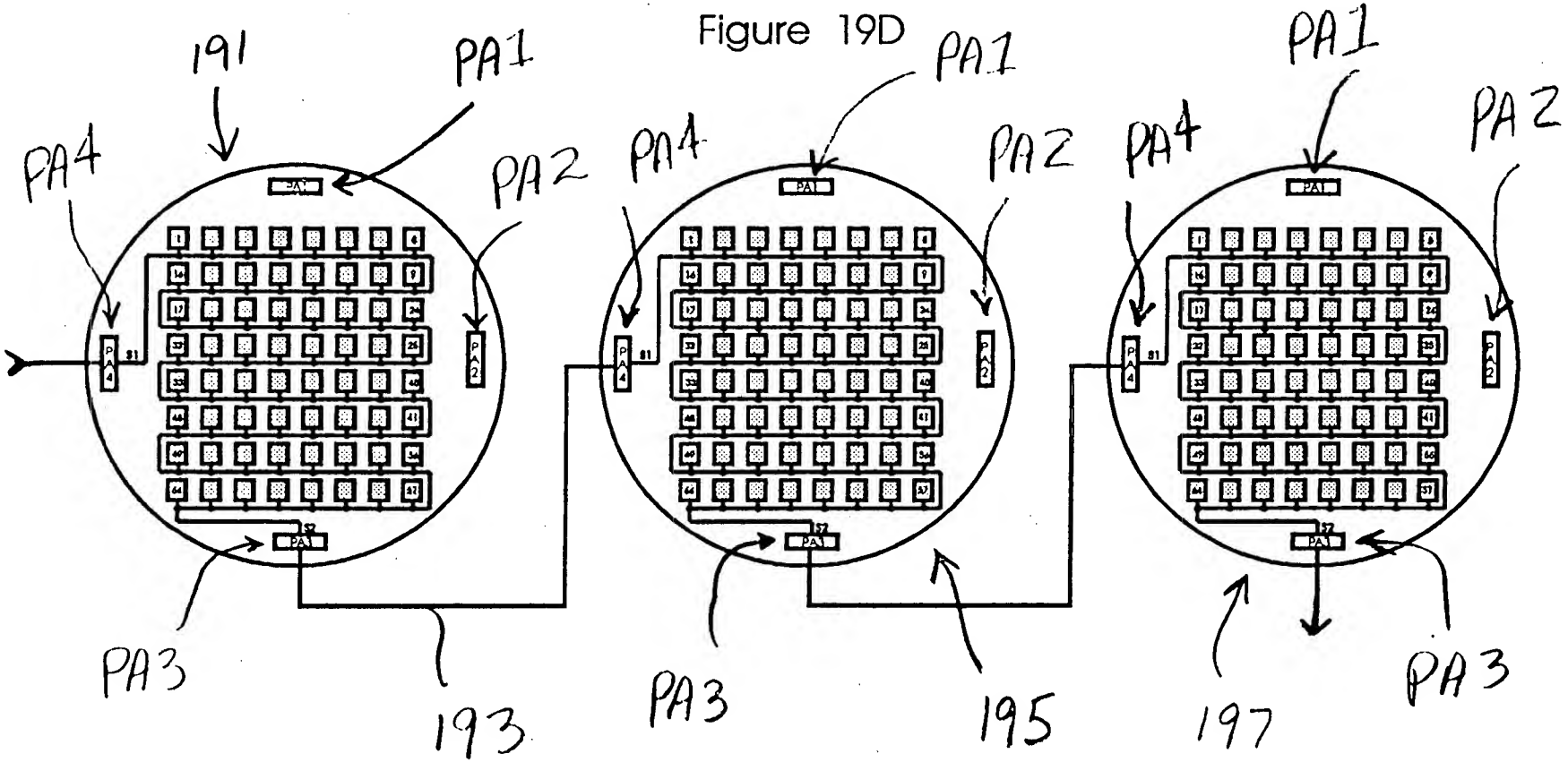


Figure 20A

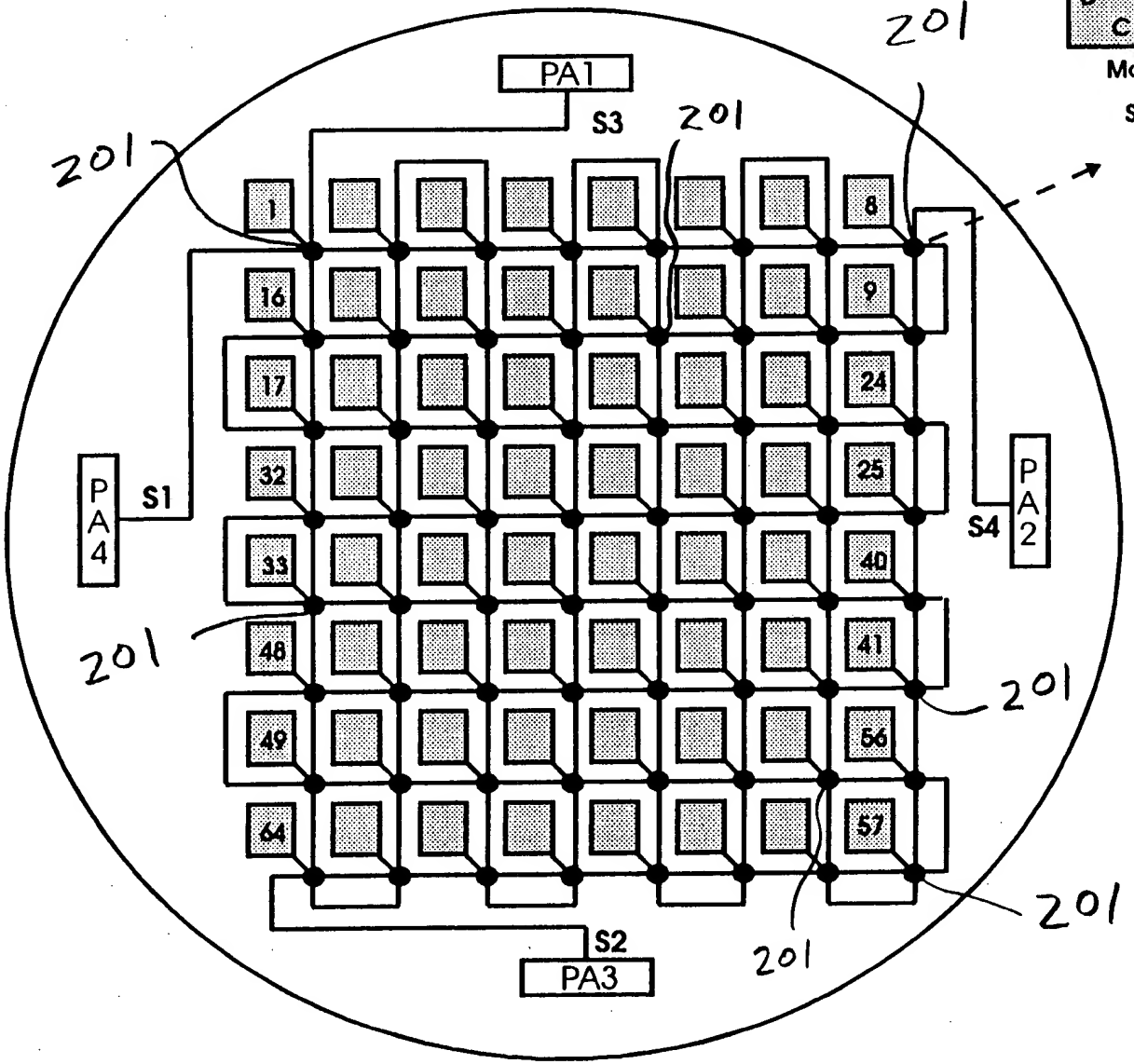


Figure 20B

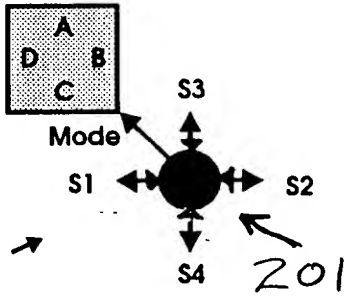


Figure 21A

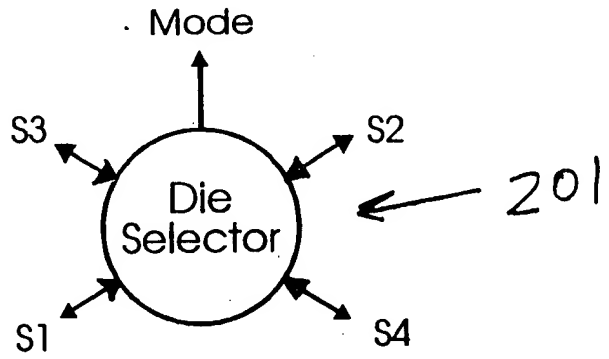


Figure 21B

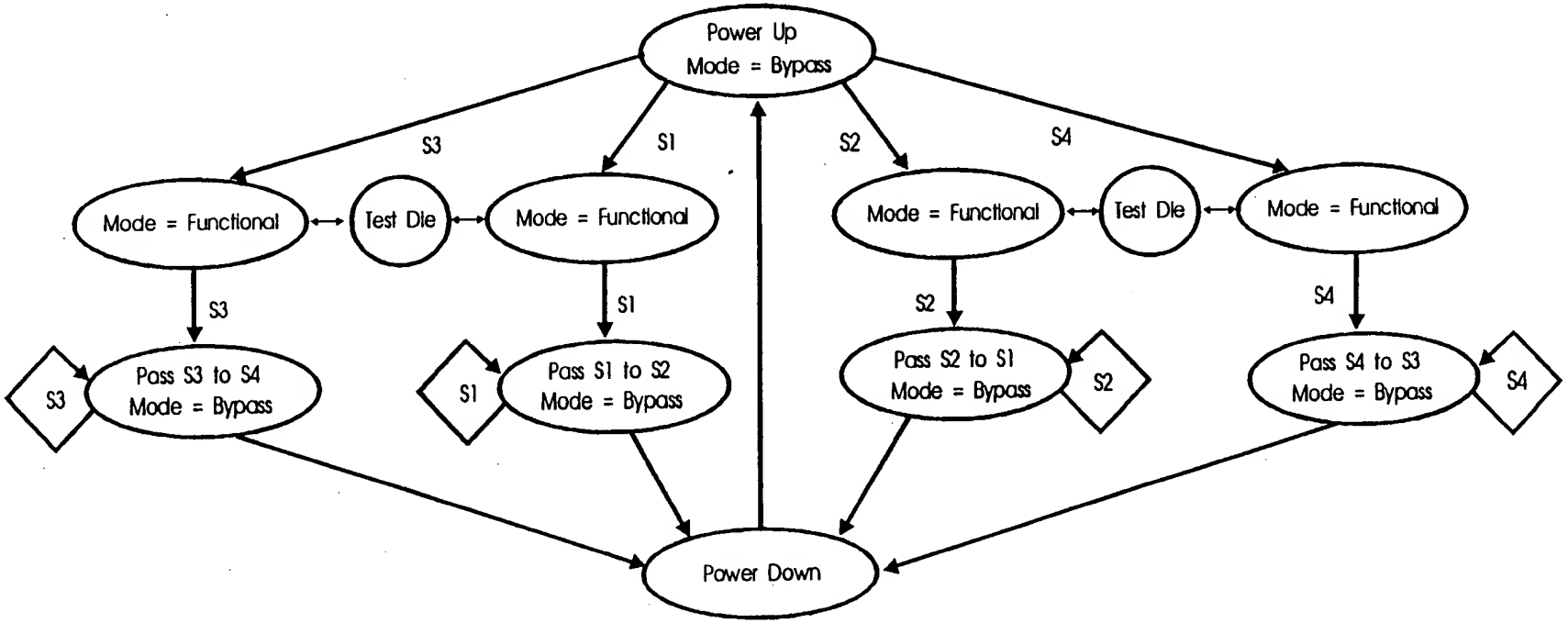


Figure 22A

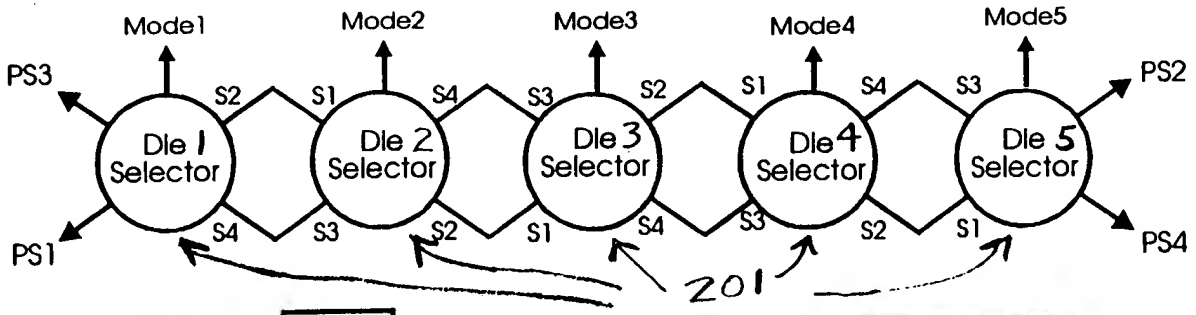


FIG. 22B

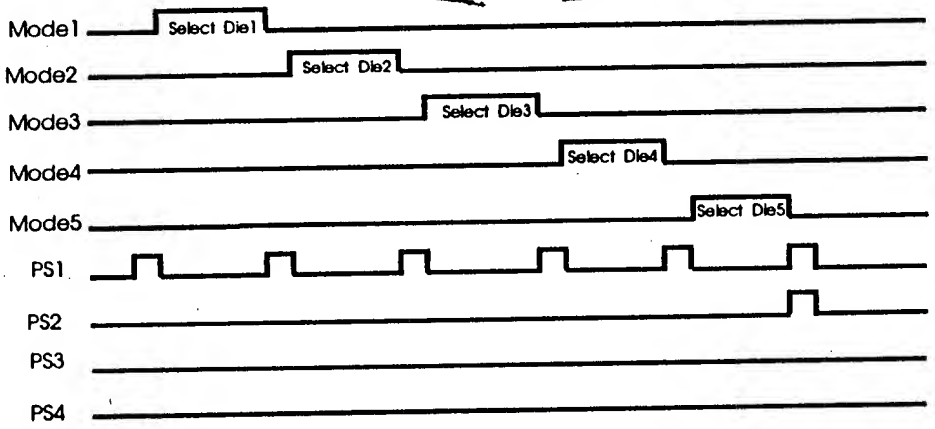
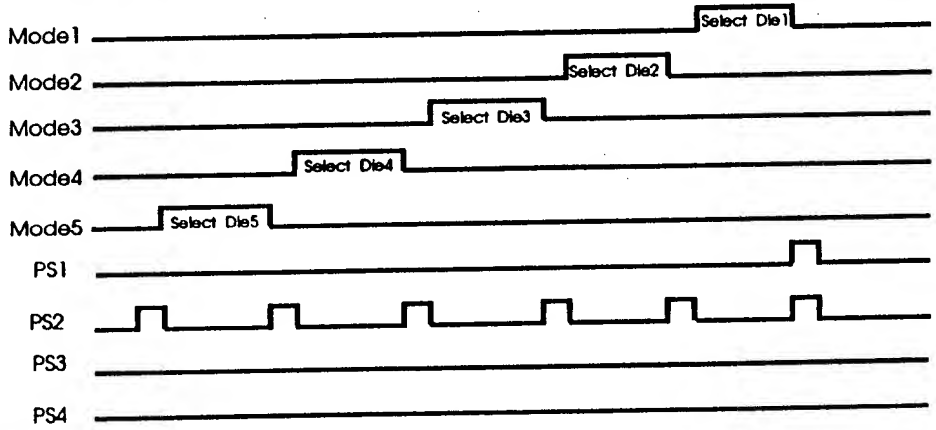


FIG. 22C



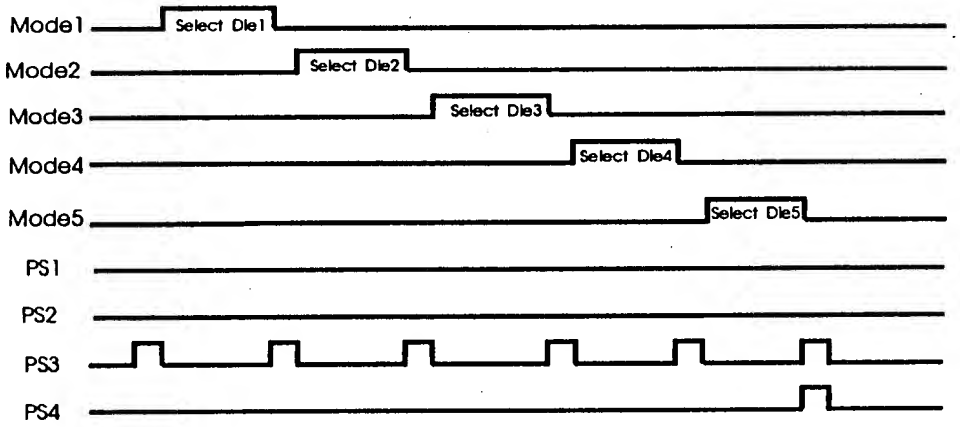


FIG. 23A

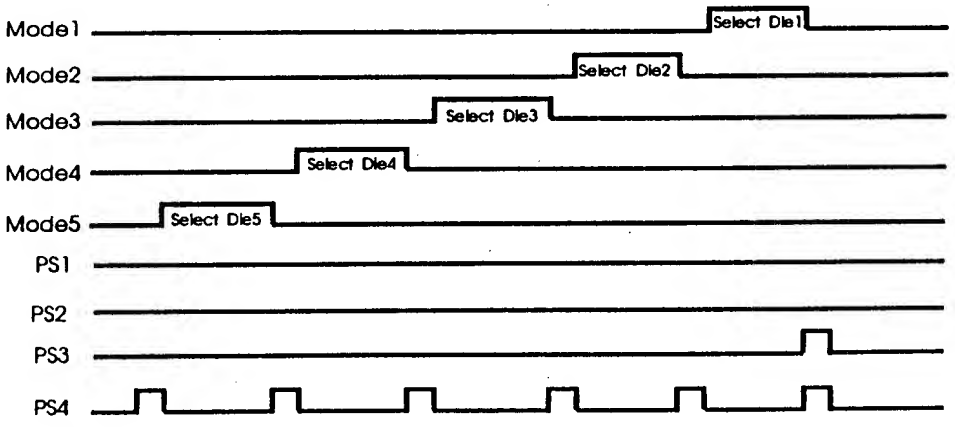


FIG. 23B

Figure 24A

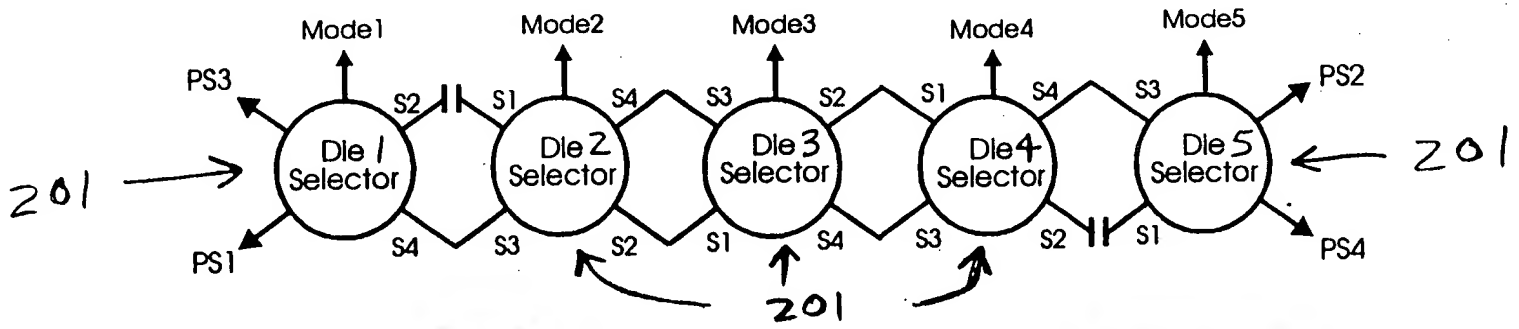


FIG. 24B

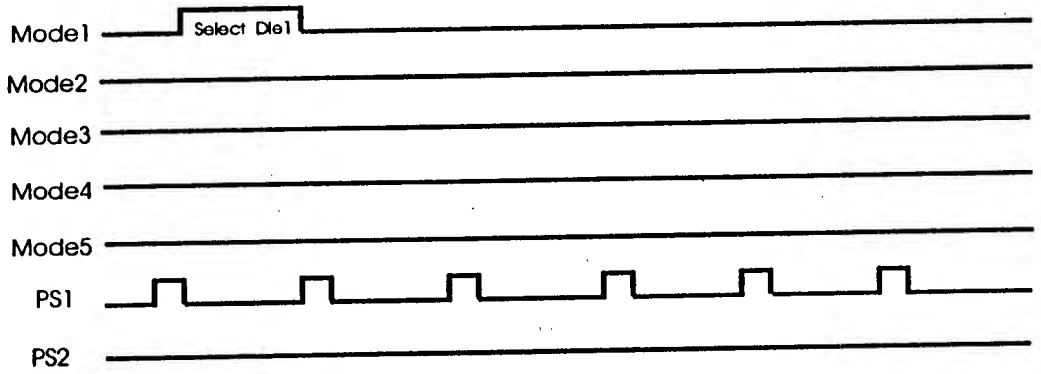


FIG. 24C

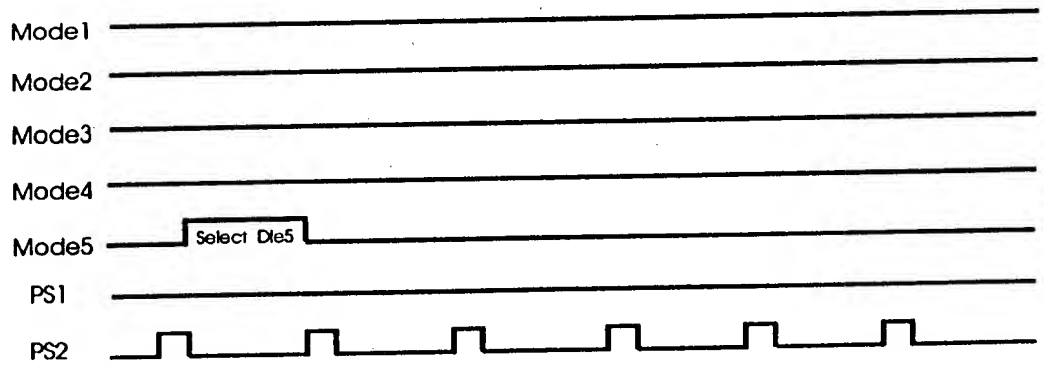


Figure 24D

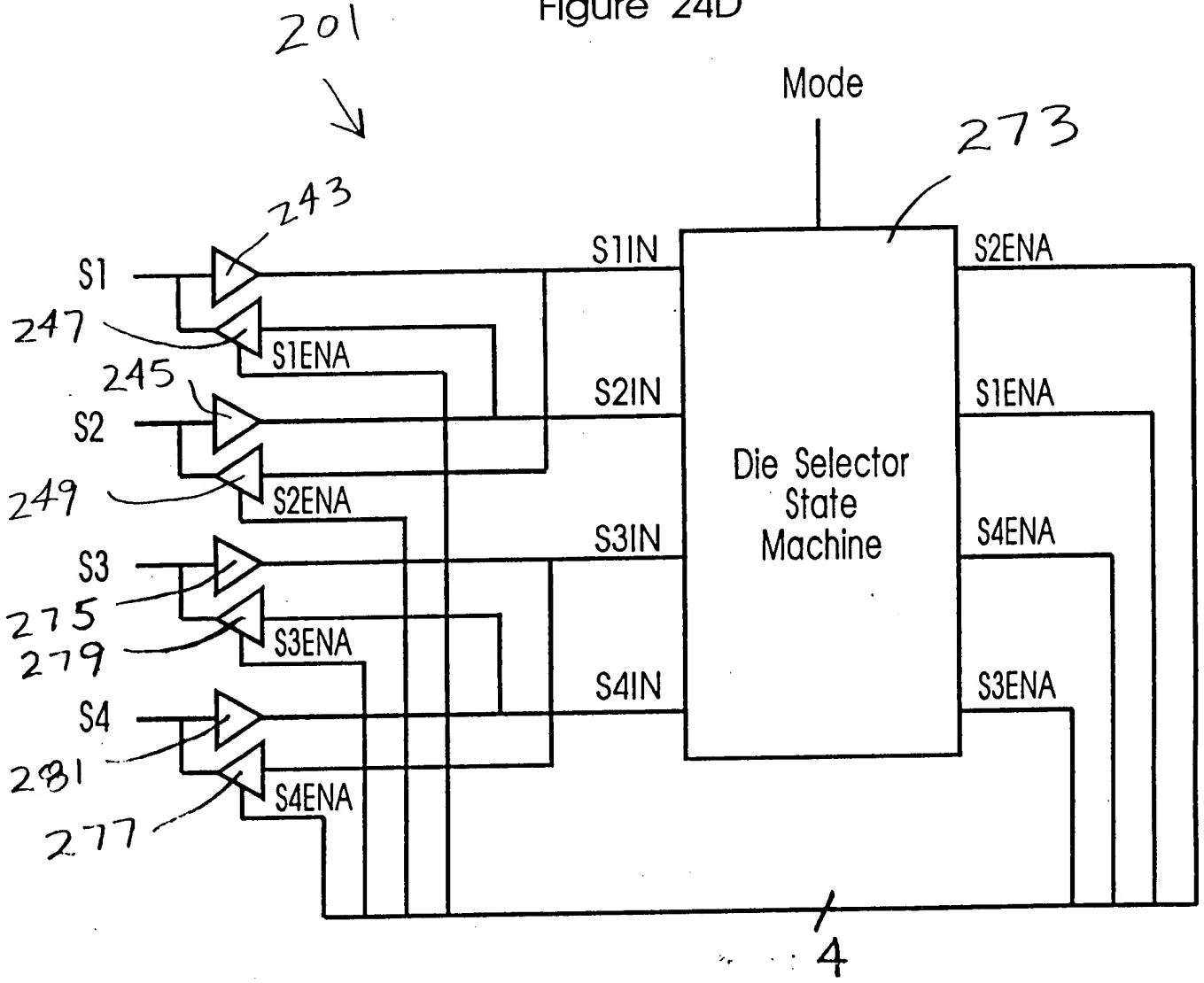

201
Mode
273
243
S1
247
S1ENA
245
S2
249
S2ENA
S3
275
279
S3ENA
S4
281
S4ENA
277
S1IN
S2IN
S3IN
S4IN
Die Selector State Machine
S2ENA
S1ENA
S4ENA
S3ENA
4

Figure 24E

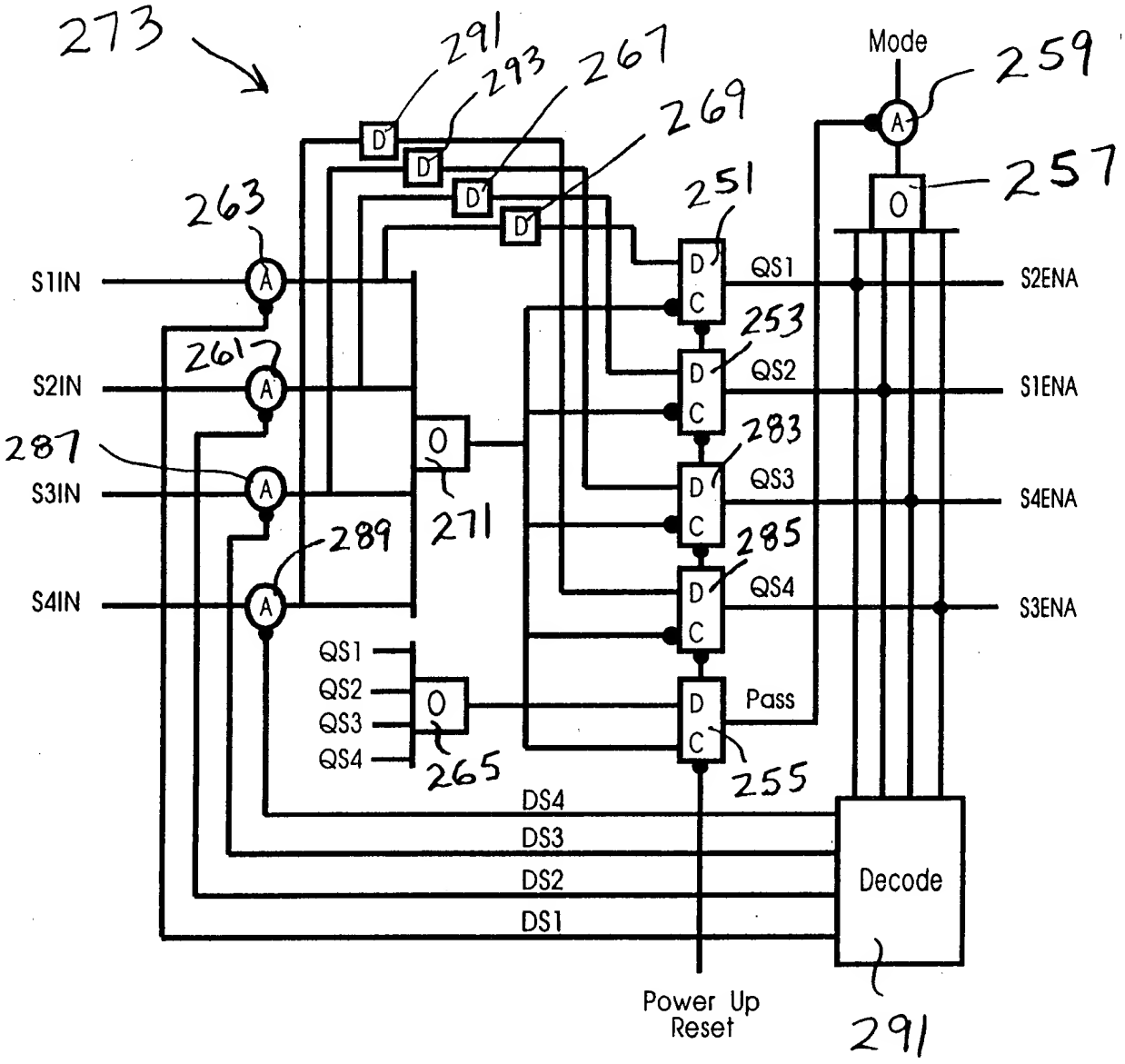

273
291
293
267
269
Mode
259
257
263
251
S1IN
S2IN
S3IN
S4IN
261
287
289
271
265
255
291
QS1
QS2
QS3
QS4
Pass
S1ENA
S2ENA
S3ENA
S4ENA
DS4
DS3
DS2
DS1
Decode
Power Up
Reset

Figure 24F

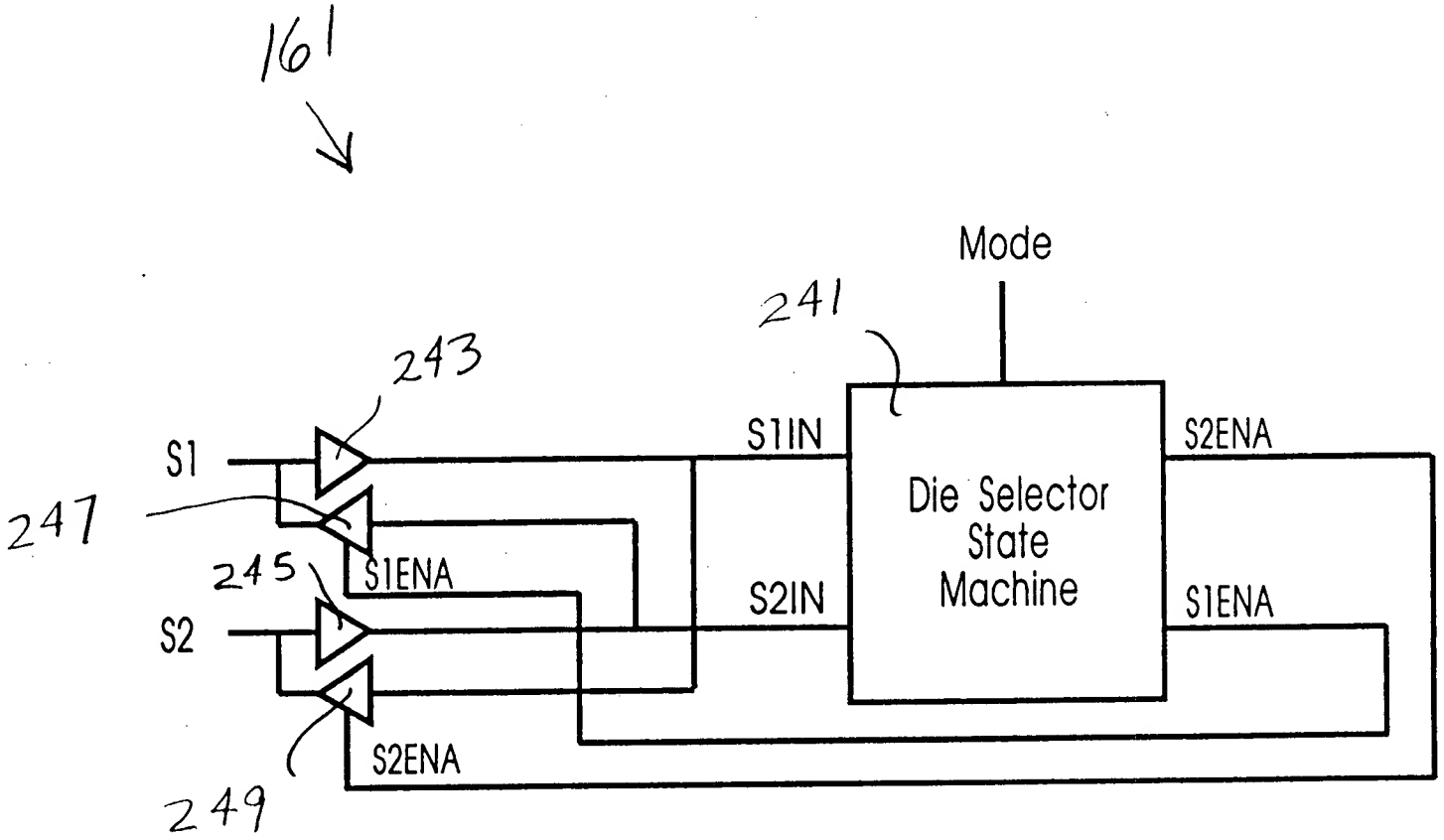

161
Mode
241
243
S1
247
S1IN
S2ENA
Die Selector
State
Machine
245
S1ENA
S2IN
S2
S1ENA
S2ENA
249

Figure 24G

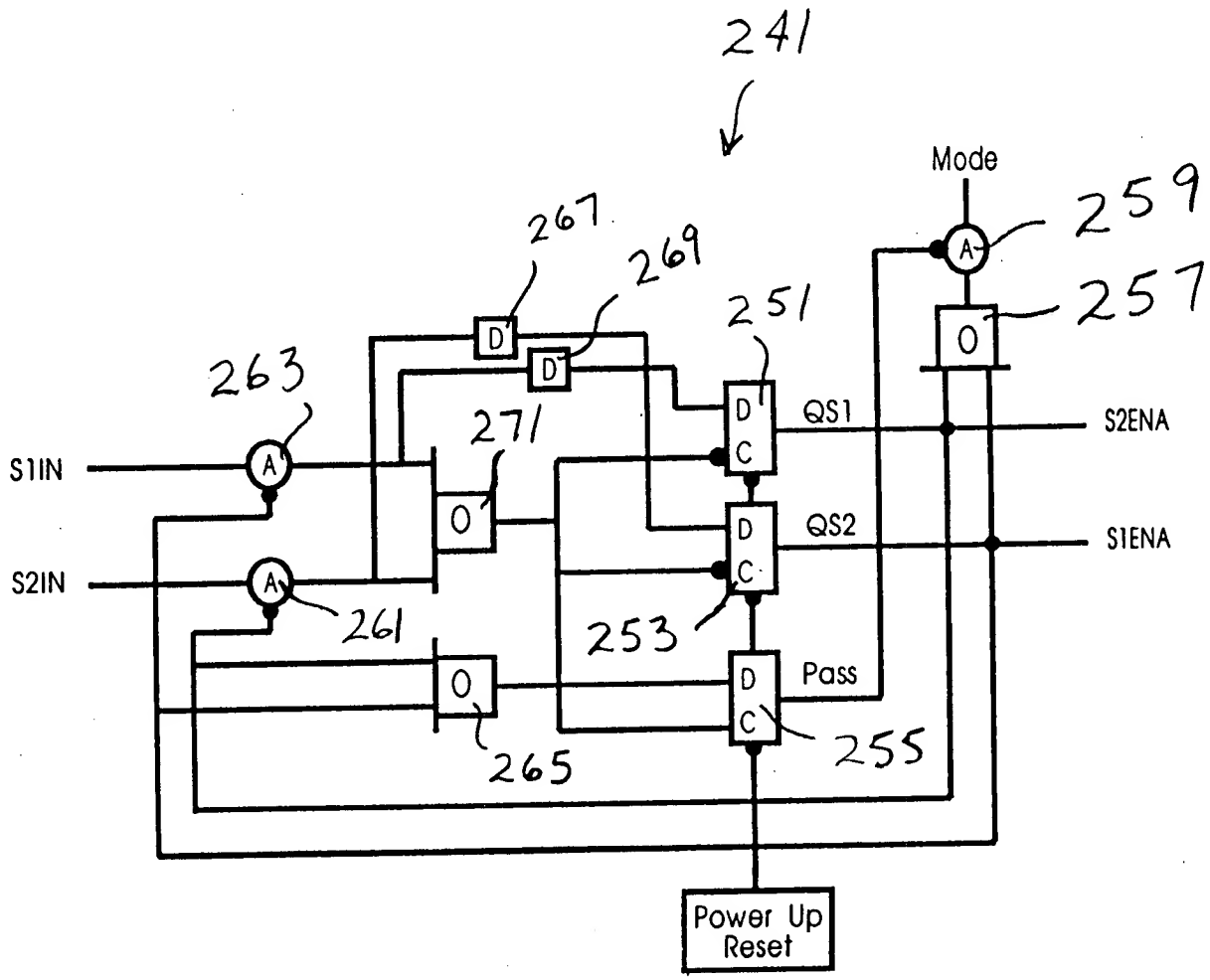

241
Mode
259
257
267
269
251
263
271
S1IN
S2IN
261
253
265
255
QS1
QS2
Pass
S2ENA
S1ENA
Power Up Reset

Figure 25A

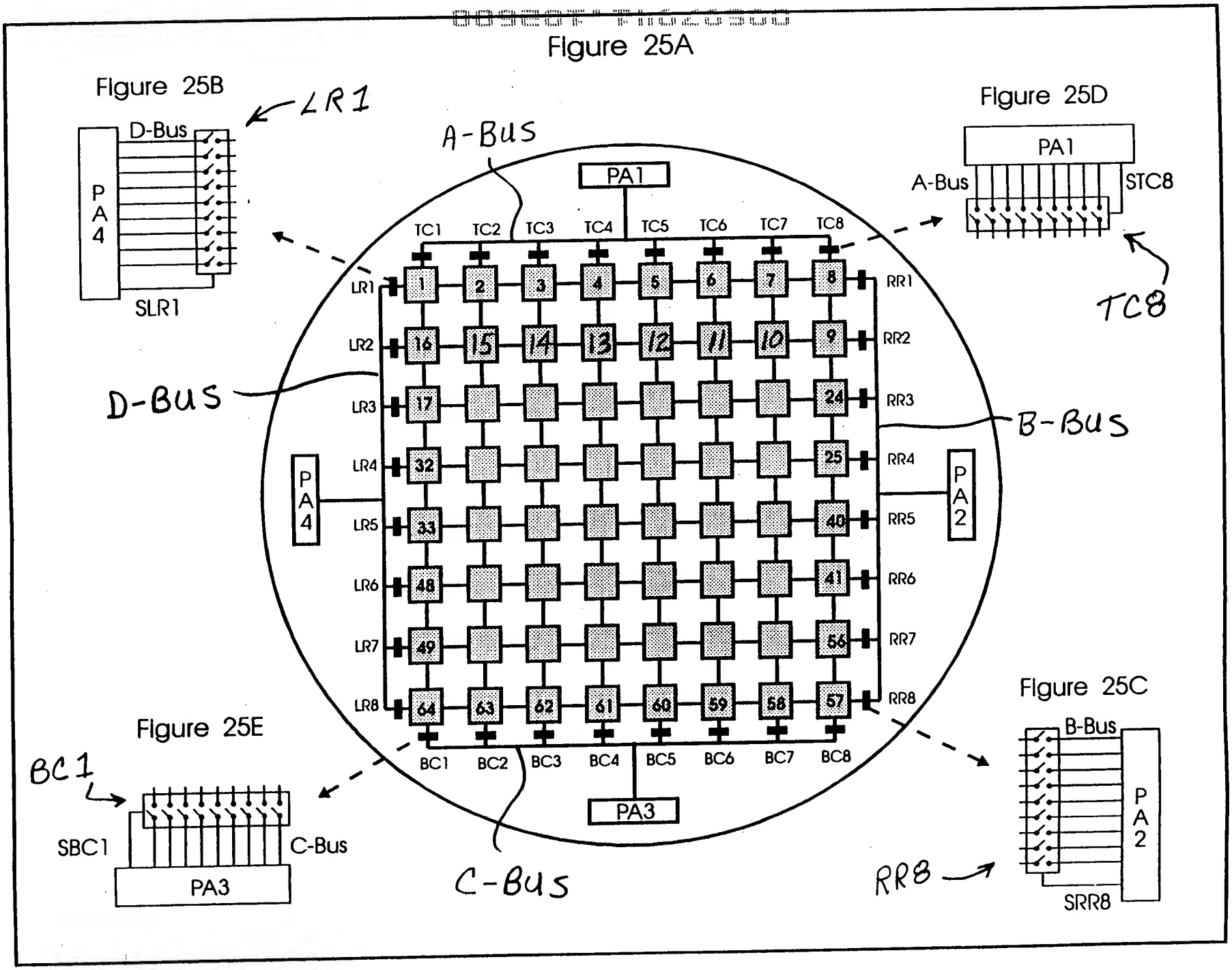


Figure 25B
LR1
D-Bus
PA4
SLR1
A-Bus
PA1
TC1 TC2 TC3 TC4 TC5 TC6 TC7 TC8
LR1 LR2 LR3 LR4 LR5 LR6 LR7 LR8
1 2 3 4 5 6 7 8
16 15 14 13 12 11 10 9
17 24
32 25
33 40
48 41
49 56
64 63 62 61 60 59 58 57
RR1 RR2 RR3 RR4 RR5 RR6 RR7 RR8
D-Bus
B-Bus
PA4
PA2
BC1 BC2 BC3 BC4 BC5 BC6 BC7 BC8
PA3
C-Bus
Figure 25D
PA1
A-Bus
STC8
TC8
Figure 25C
B-Bus
PA2
RR8
SRR8
Figure 25E
BC1
SBC1
C-Bus
PA3

Figure 26

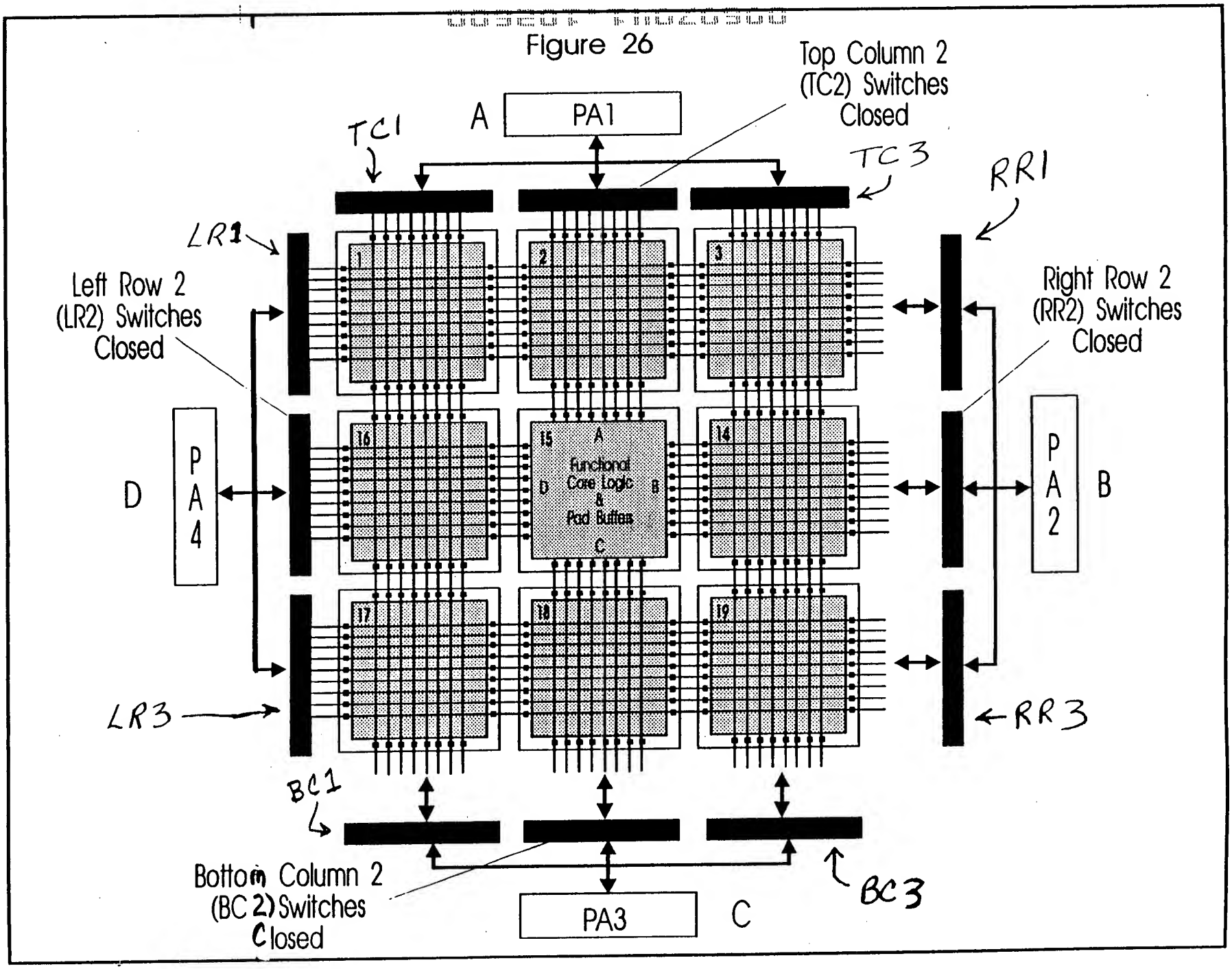
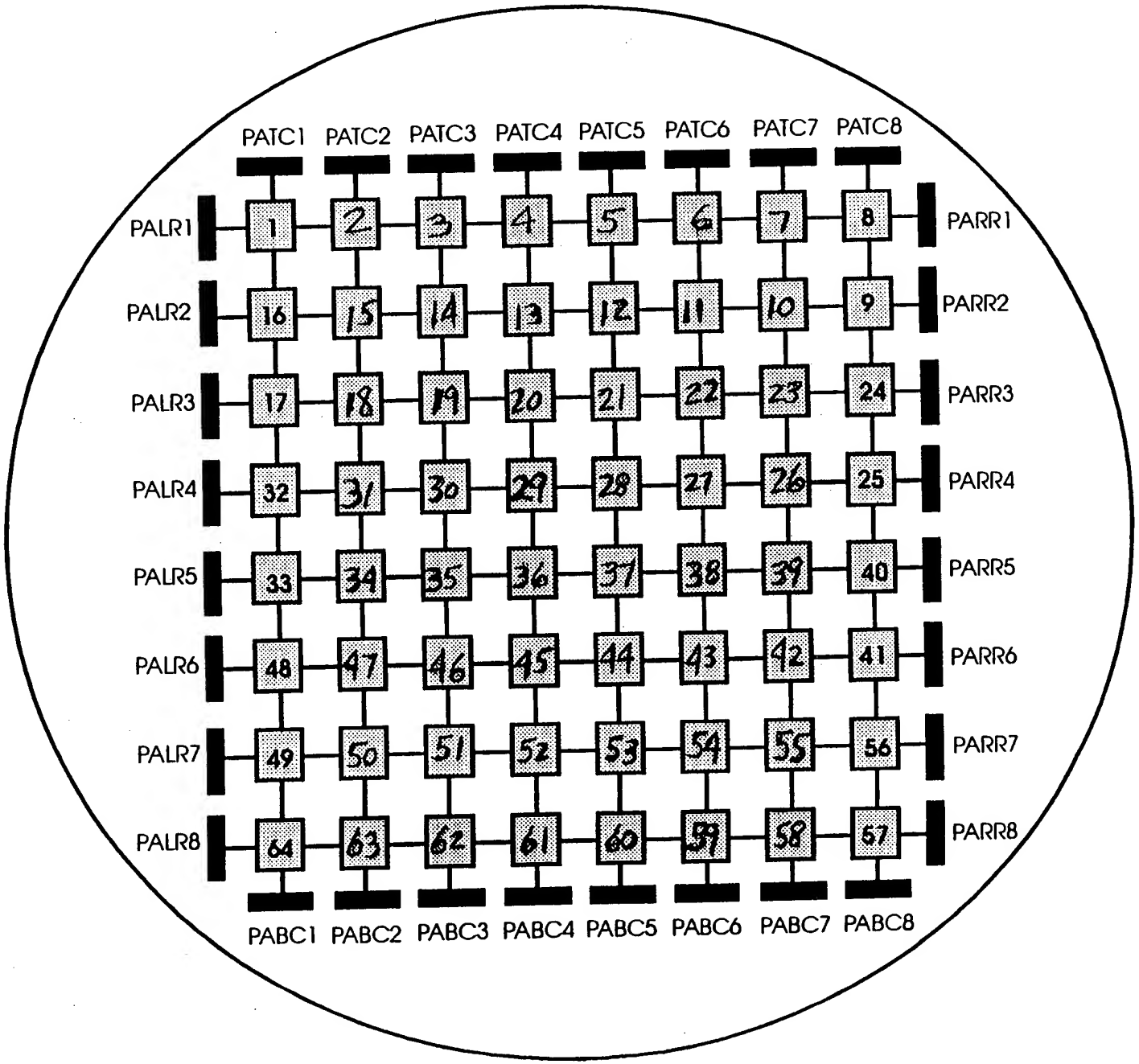

Top Column 2
(TC2) Switches
Closed
A
PA1
TC1
TC3
RR1
LR1
Left Row 2
(LR2) Switches
Closed
Right Row 2
(RR2) Switches
Closed
1
2
3
16
15
A
Functional
Core Logic
&
Pad Buffers
D
B
C
14
D
PA
4
PA
2
B
17
18
19
LR3
RR3
BC1
Bottom Column 2
(BC 2) Switches
Closed
PA3
C
BC3

Figure 27


PATC1
PATC2
PATC3
PATC4
PATC5
PATC6
PATC7
PATC8
PALR1
PALR2
PALR3
PALR4
PALR5
PALR6
PALR7
PALR8
PARR1
PARR2
PARR3
PARR4
PARR5
PARR6
PARR7
PARR8
PABC1
PABC2
PABC3
PABC4
PABC5
PABC6
PABC7
PABC8
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
17
18
19
20
21
22
23
24
32
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64
63
62
61
60
59
58
57

Figure 28

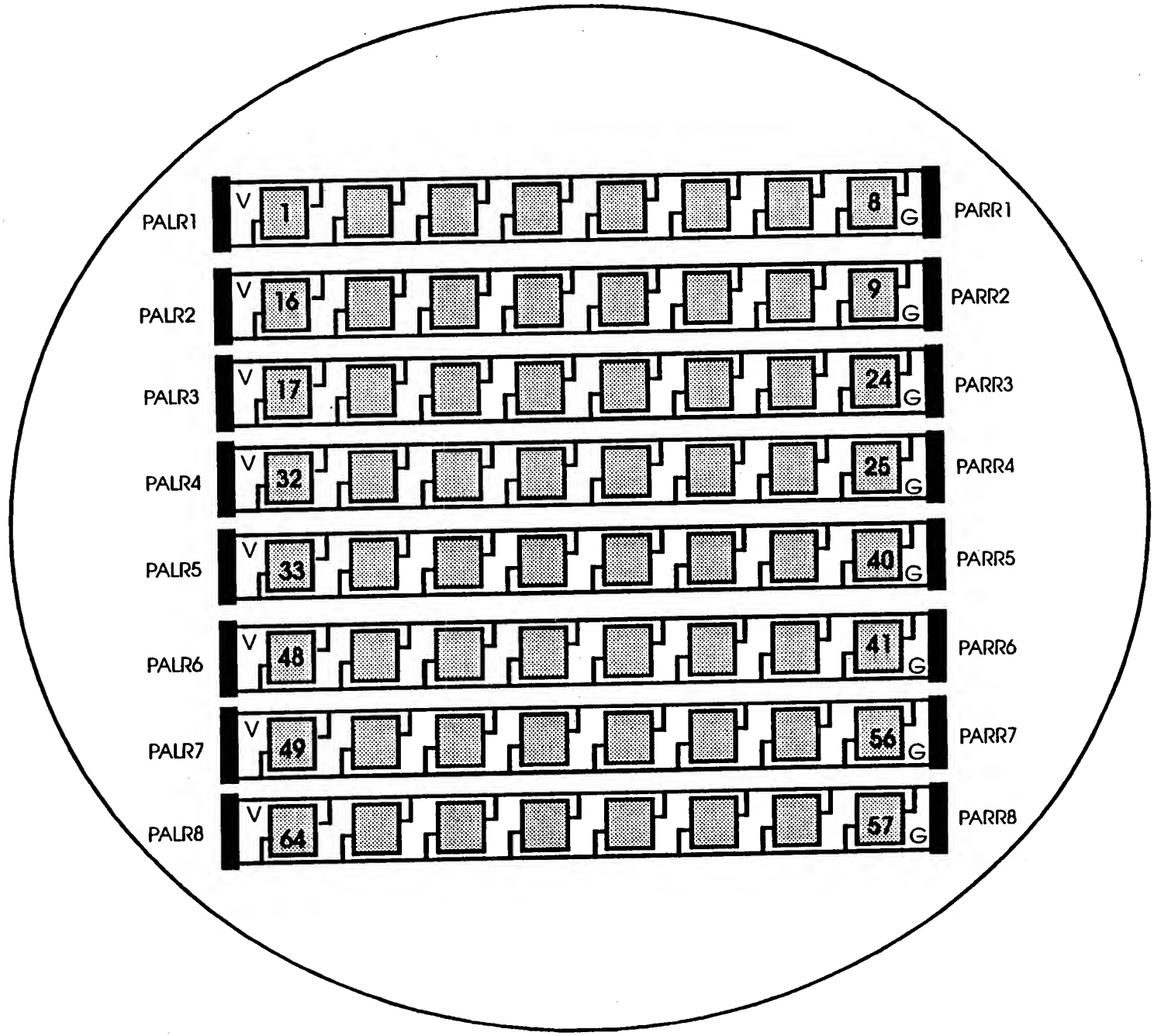

PALR1
V
1
8
G
PARR1
PALR2
V
16
9
G
PARR2
PALR3
V
17
24
G
PARR3
PALR4
V
32
25
G
PARR4
PALR5
V
33
40
G
PARR5
PALR6
V
48
41
G
PARR6
PALR7
V
49
56
G
PARR7
PALR8
V
64
57
G
PARR8

Figure 29

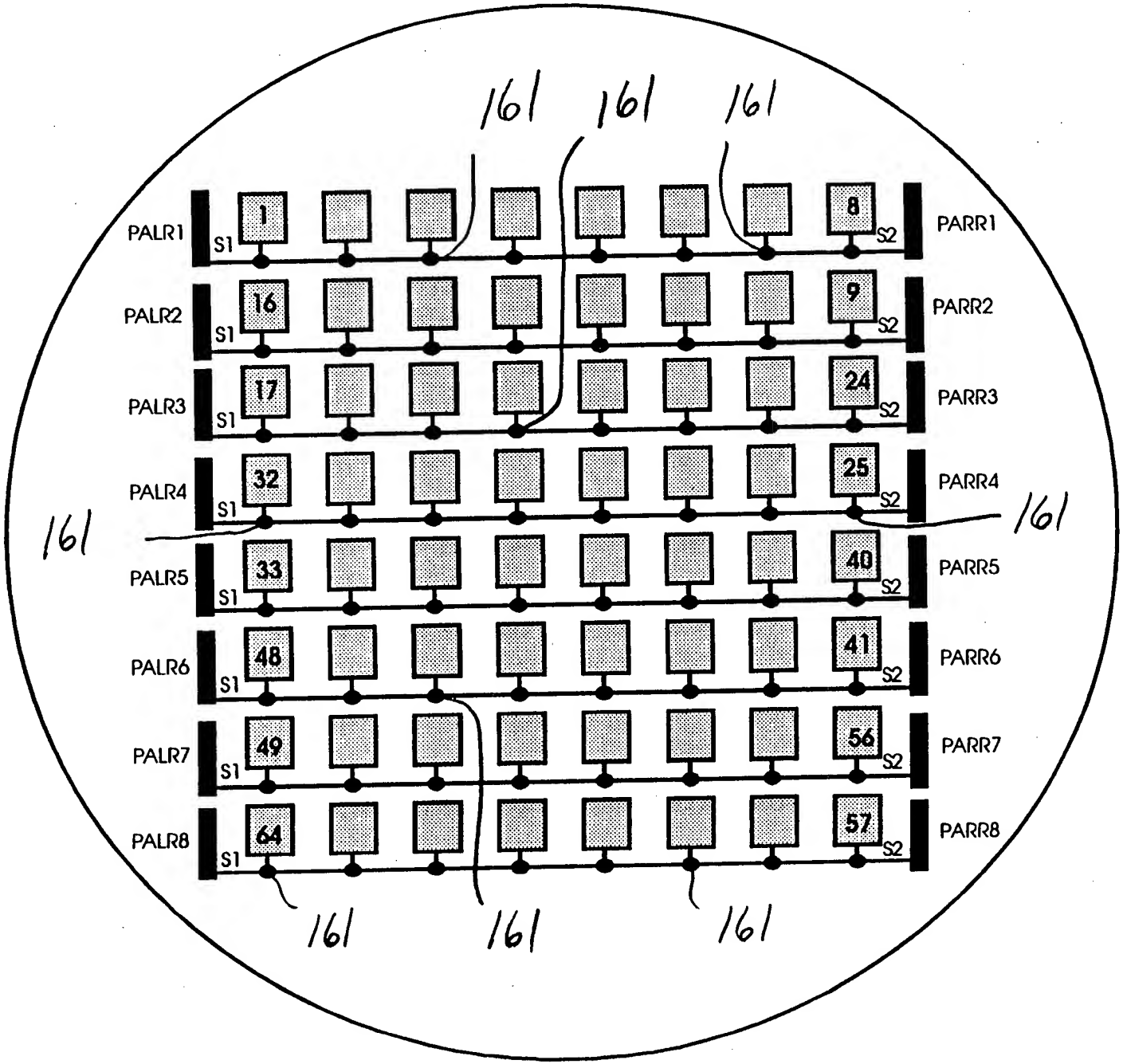

161
161
161
PALR1
PALR2
PALR3
PALR4
PALR5
PALR6
PALR7
PALR8
S1
1
16
17
32
33
48
49
64
8
9
24
25
40
41
56
57
S2
PARR1
PARR2
PARR3
PARR4
PARR5
PARR6
PARR7
PARR8
161
161
161
161
161
161

Figure 30

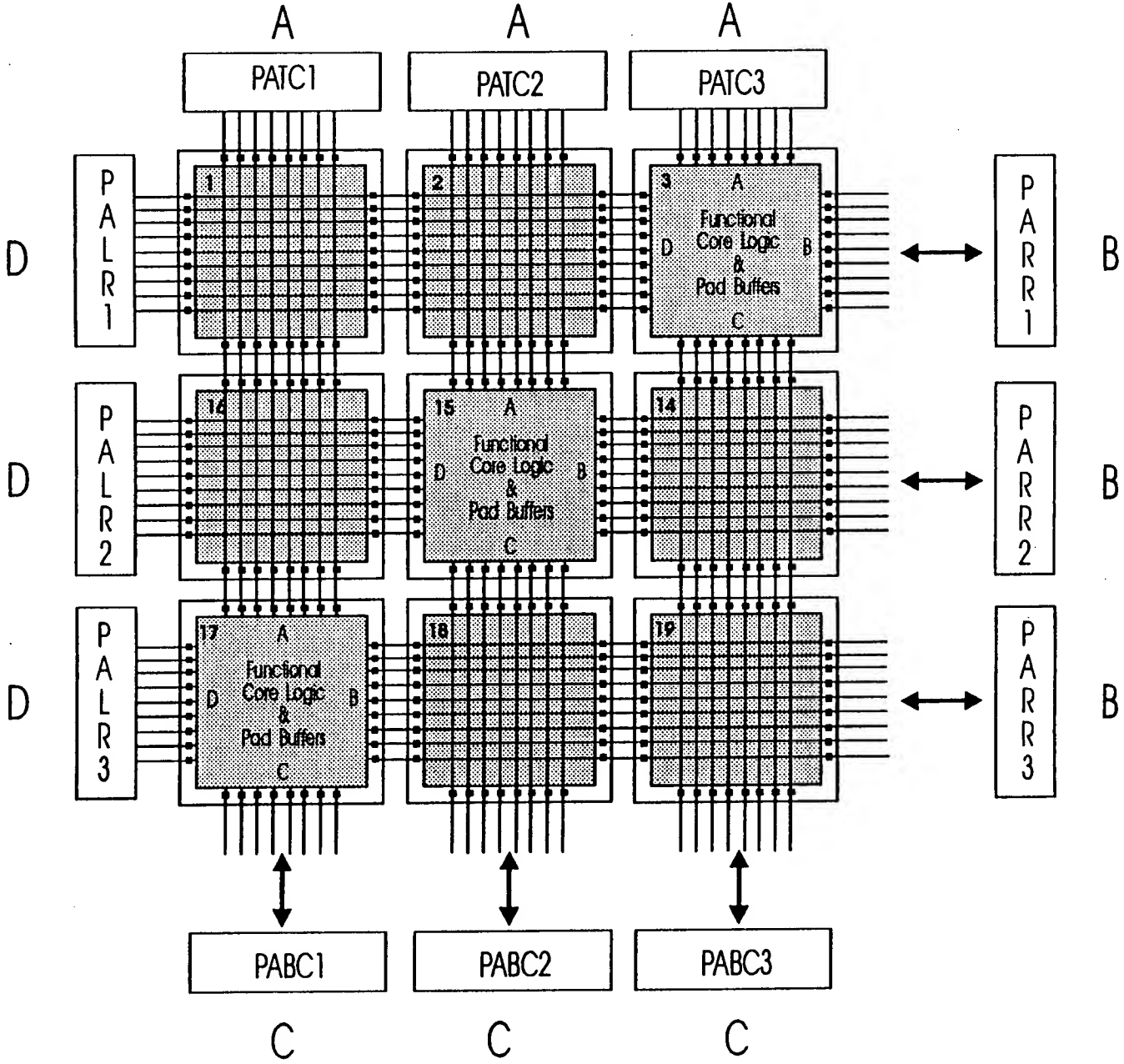

A
A
A
PATC1
PATC2
PATC3
PALR1
PALR2
PALR3
PARR1
PARR2
PARR3
D
D
D
B
B
B
1
2
3
A
Functional
Core Logic
&
Pad Buffers
D
B
C
14
15
A
Functional
Core Logic
&
Pad Buffers
D
B
C
14
17
A
Functional
Core Logic
&
Pad Buffers
D
B
C
18
19
PABC1
PABC2
PABC3
C
C
C

Figure 31A

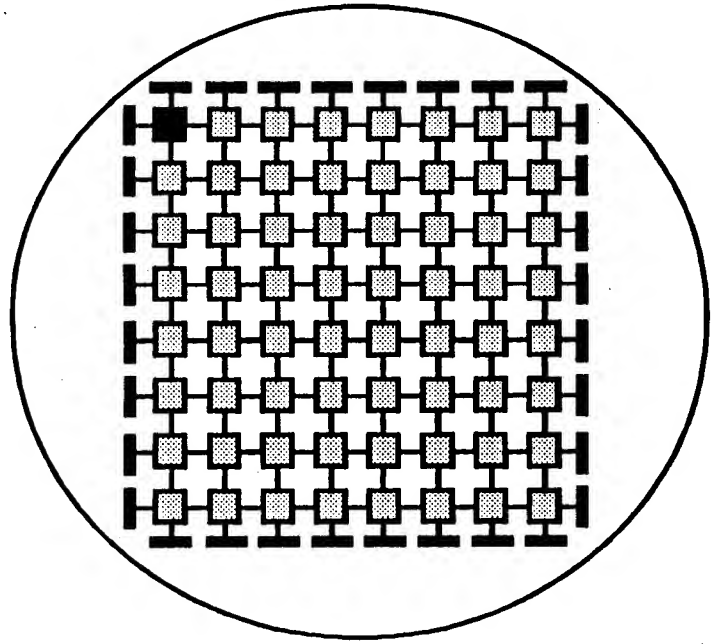


Figure 31B

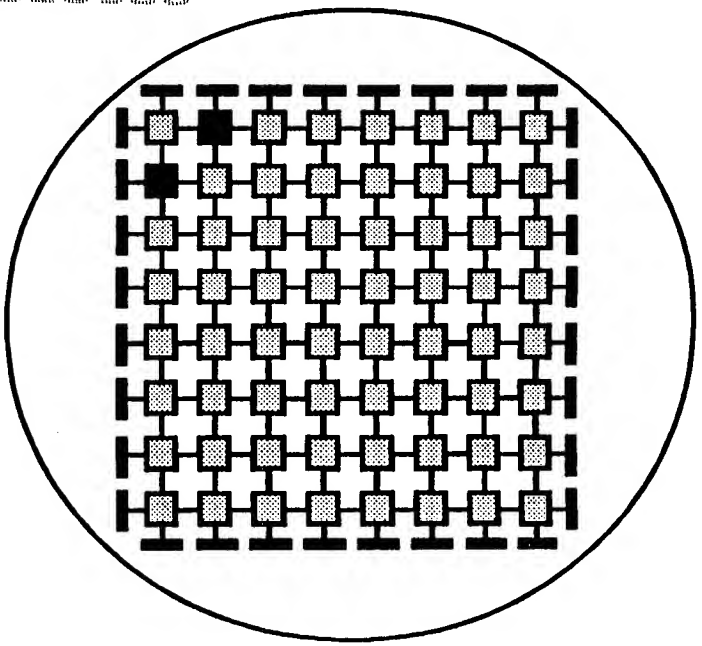


Figure 31C

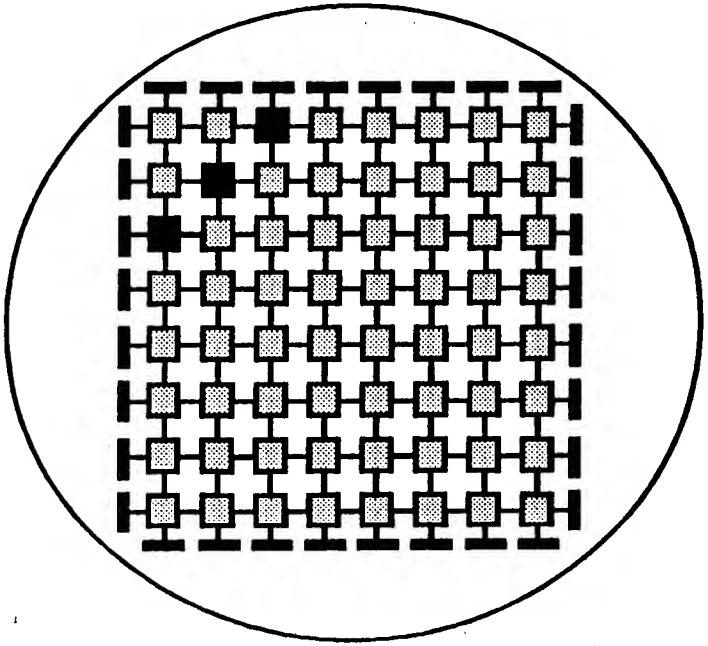


Figure 31D

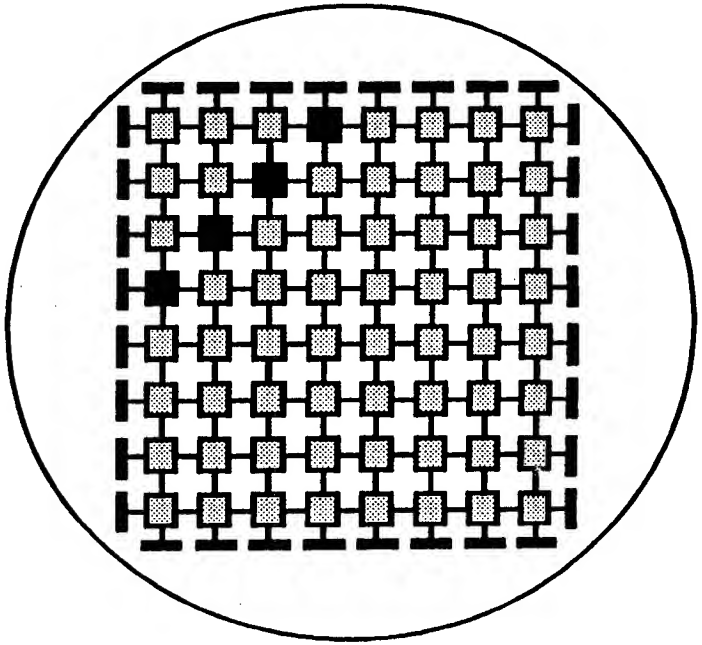


Figure 31E

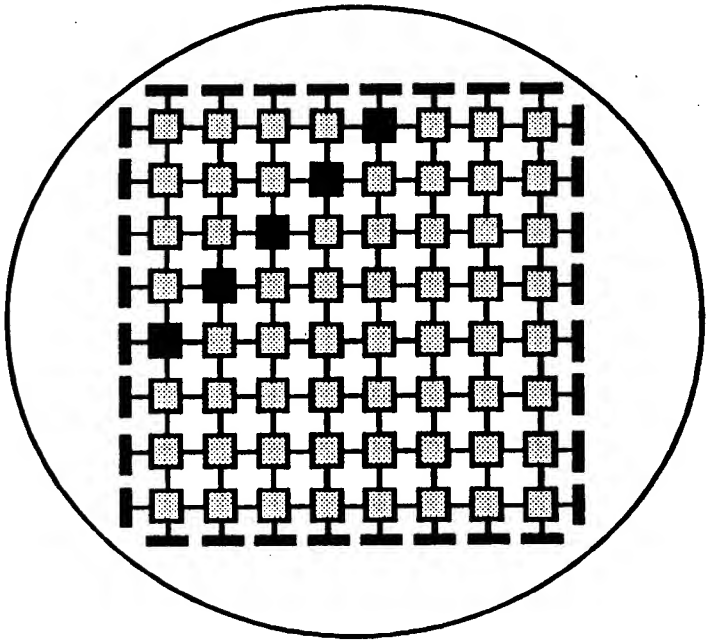


Figure 31F

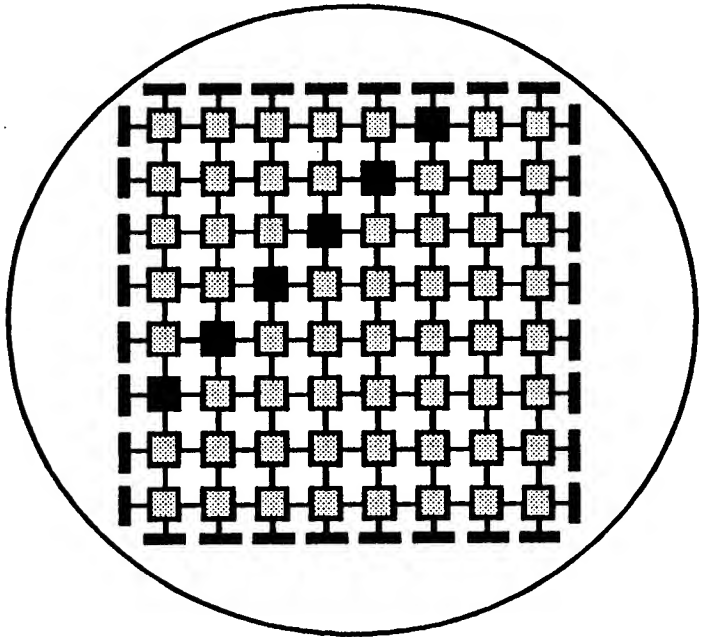


Figure 31G

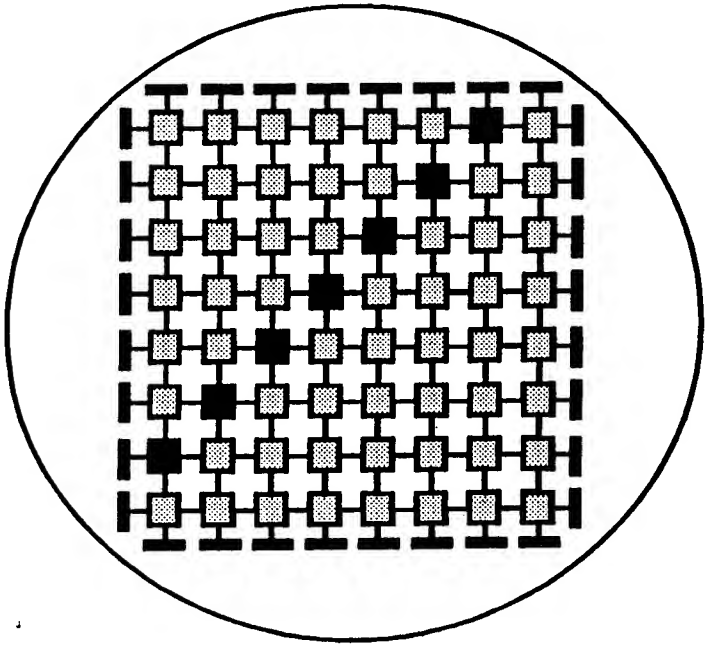


Figure 31H

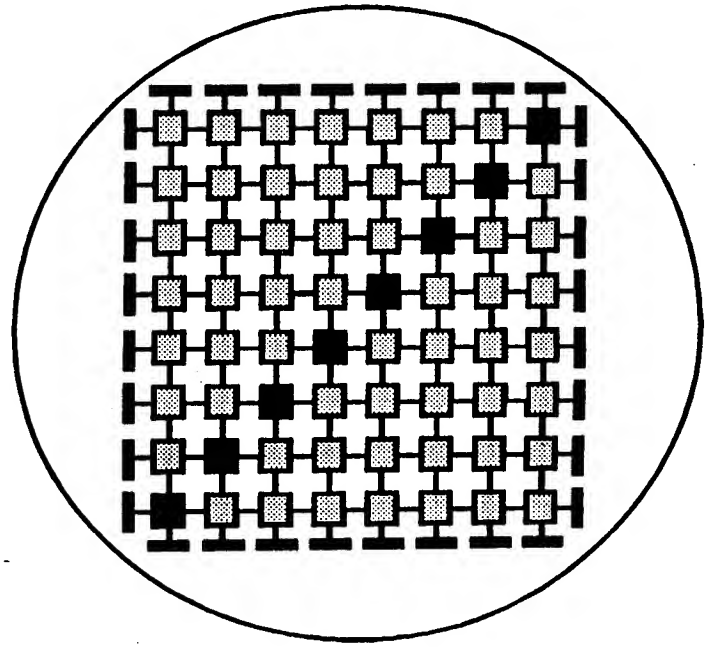


Figure 31I

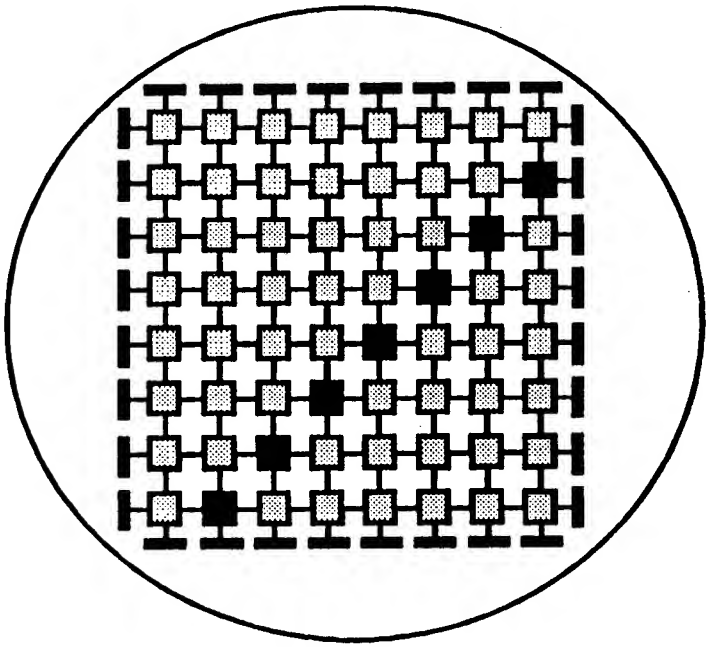


Figure 31J

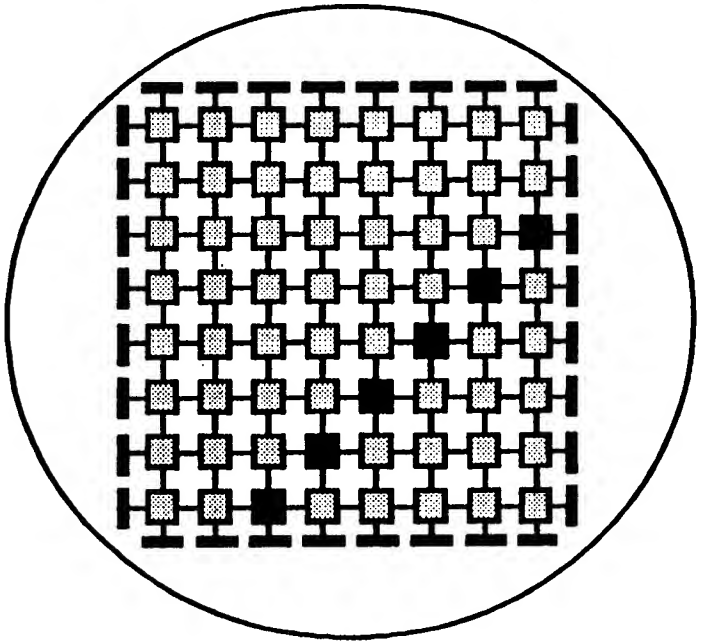


Figure 31K

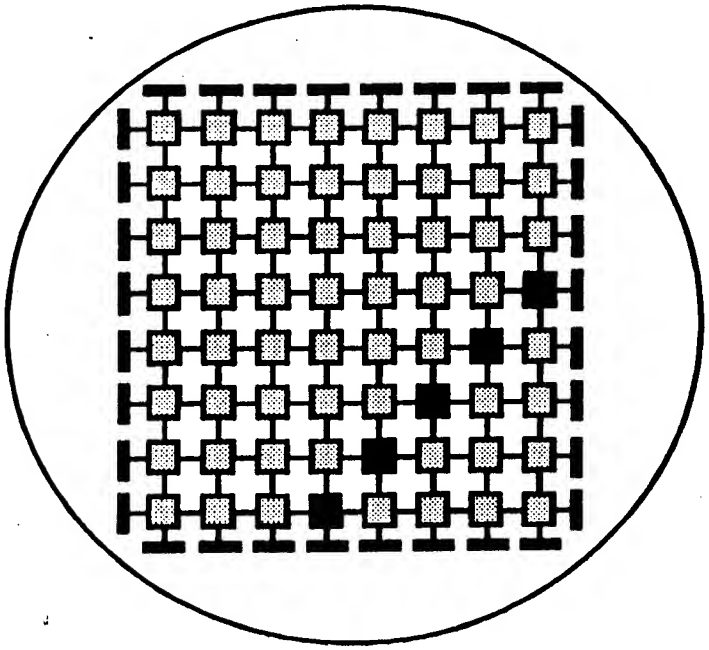


Figure 31L

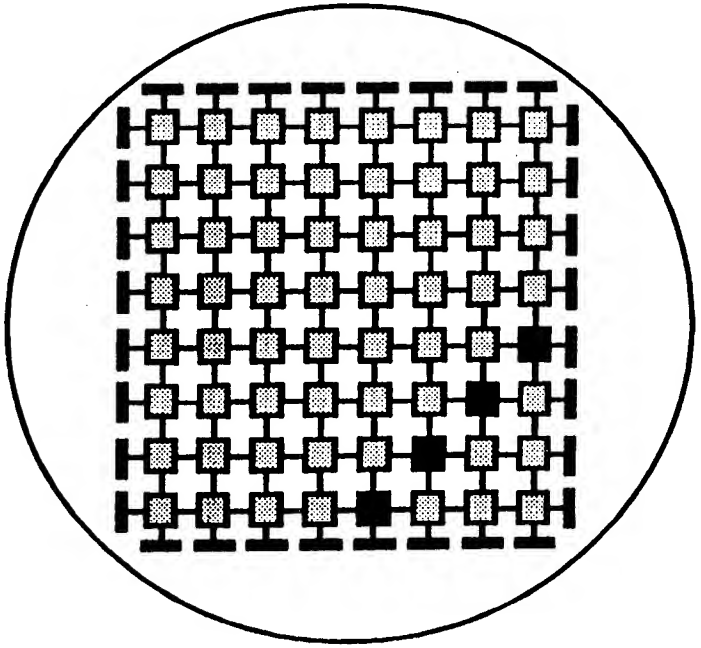


Figure 31M

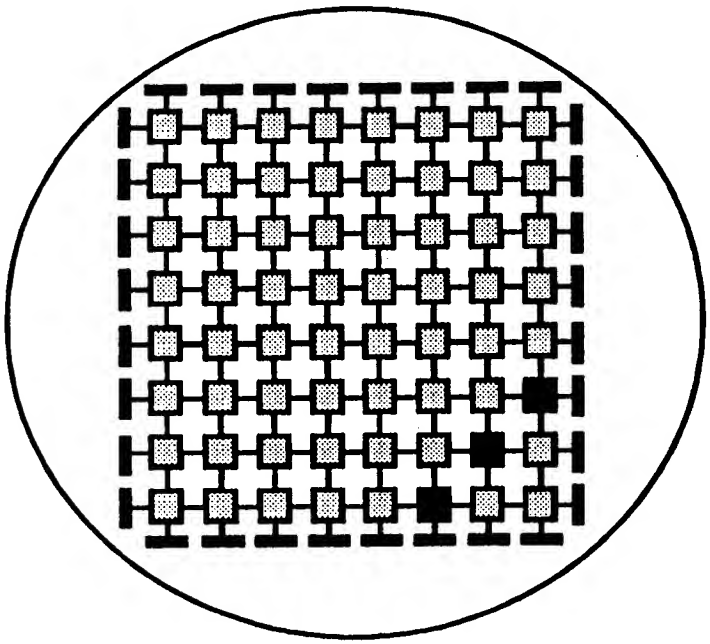


Figure 31N

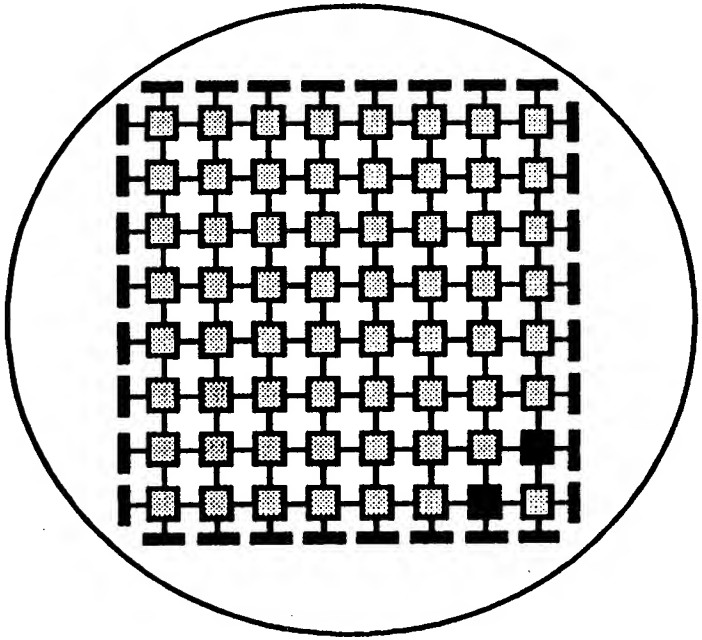


Figure 31O

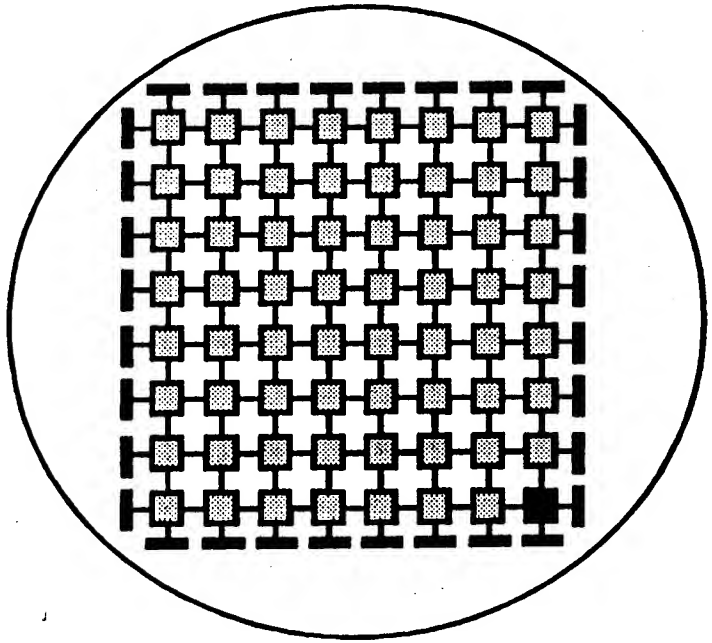
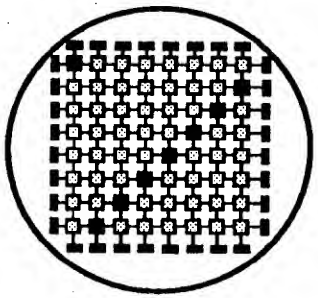
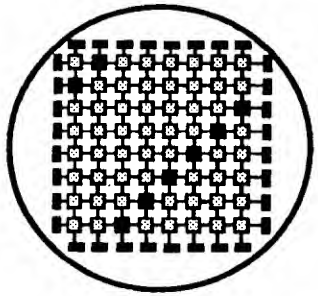


Figure 32A



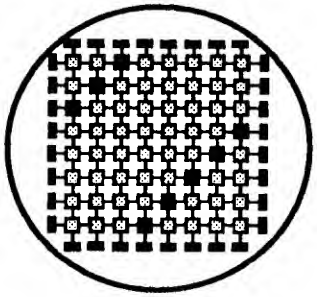
Test Steps
1 & 9

Figure 32B



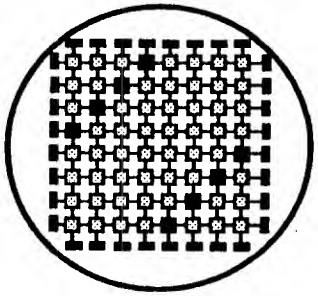
Test Steps
2 & 10

Figure 32C



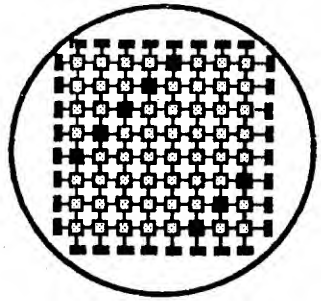
Test Steps
3 & 11

Figure 32D



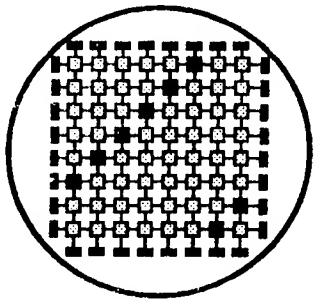
Test Steps
4 & 12

Figure 32E



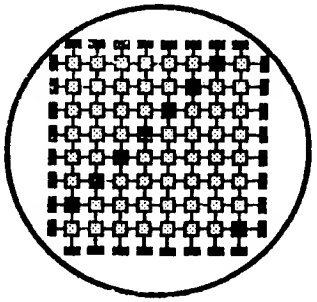
Test Steps
5 & 13

Figure 32F



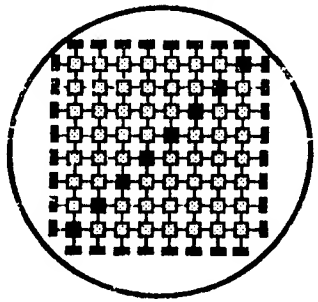
Test Steps
6 & 14

Figure 32G



Test Steps
7 & 15

Figure 32H



Test Step
8